Attorney Docket No. **09792909-5696** PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Patent Application of:	)	Group Art Unit: 2891
	)	
Hideo Yamanaka	)	Examiner: Bradley Smith
	)	
Application No. **10/680,548**	)	
	)	
Filed: **October 7, 2003**	)	
	)	
For: METHOD FOR PRODUCING ULTRA-THIN SEMICONDUCTOR DEVICE	)	

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPELLANT'S BRIEF ON APPEAL

Dear Sir:

In accordance with the provisions of 37 C.F.R. § 41.37, Appellant herewith submits this Brief in support of the Appeal for the above-referenced application.

I. REAL PARTY IN INTEREST

The real party in interest in the present appeal is the Assignee, Sony Corporation, a Japanese Corporation. The Assignment was recorded in the U.S. Patent and Trademark Office at Reel 015335, Frame 0984 on May 17, 2004.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals and no related interferences.

III. STATUS OF CLAIMS

Claims 1-84 are pending in this application, and claims 2-83 have been withdrawn from consideration. The present Appeal is directed to claims 1 and 84 that were rejected under 35 U.S.C. § 103(a) as being unpatentable over Yonehara et al. (U.S. Patent No. 5,453,394) in a final office action dated December 20, 2005.

IV. STATUS OF AMENDMENTS

There are no pending amendments. However, appellant reserves the right to submit an amendment to correct noted typographical errors that do not affect the appeal.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The present invention is directed to a method of production of an ultra-thin semiconductor device. (See page 24, line 1 through page 57, line 11). The method comprises the steps of forming a first single crystalline semiconductor layer (ref. no. 12, Fig. 2A) on a seed substrate (ref. no. 10, Fig. 2A) via a first porous semiconductor peeling layer (ref. no. 11, Fig. 2A) (see page 24, line 12 through page 33, line 9 and Fig. 2A); bonding the seed substrate from the first single crystalline semiconductor layer side in the state with an insulating layer (ref. no. 23, Figs. 2B and 3A) interposed to a support substrate (ref. no. 20, Figs. 2B and 3A) having a second single crystalline semiconductor layer (ref. no. 22, Figs. 2B and 3A) formed thereon via a second porous semiconductor peeling layer (ref. no. 21, Figs. 2B and 3A) wherein the first porous semiconductor peeling layer has a greater porosity or thickness than the second porous semiconductor peeling layer (see page 33, line 10 through page 36, line 3 and Fig. 3A);

separating the seed substrate using the first porous semiconductor peeling layer as an interface (see page 35, line 19 through page 39, line 8 and Fig. 3B); and separating the support substrate using the second porous semiconductor peeling layer as an interface to obtain the first single crystalline semiconductor layer formed on the insulating layer (see page 47, line 7 through page 50, line 6 and Fig. 6B).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1 and 84 stand rejected under 35 U.S.C. § 103(a) as obvious over Yonehara et al. (U.S. Patent No. 5,453,394).

VII. ARGUMENT

Claims 1 and 84 are patentable over Yonehara et al.

A. The Claimed Invention

Claim 1 is directed to a method of production of an ultra-thin semiconductor device. The method comprises the steps of forming a first single crystalline semiconductor layer on a seed substrate via a first porous semiconductor peeling layer; bonding the seed substrate from the first single crystalline semiconductor layer side in the state with an insulating layer interposed to a support substrate having a second single crystalline semiconductor layer formed thereon via a second porous semiconductor peeling layer wherein the first porous semiconductor peeling layer has a greater porosity than the second porous semiconductor peeling layer; separating the seed substrate using the first porous semiconductor peeling layer as an interface; and separating the

support substrate using the second porous semiconductor peeling layer as an interface to obtain the first single crystalline semiconductor layer formed on the insulating layer.

Claim 84 is directed to a method of production of an ultra-thin semiconductor device. The method comprises the steps of forming a first single crystalline semiconductor layer on a seed substrate via a first porous semiconductor peeling layer; bonding the seed substrate from the first single crystalline semiconductor layer side in the state with an insulating layer interposed to a support substrate having a second single crystalline semiconductor layer formed thereon via a second porous semiconductor peeling layer wherein the first porous semiconductor peeling layer has a greater thickness than the second porous semiconductor peeling layer; separating the seed substrate using the first porous semiconductor peeling layer as an interface; and separating the support substrate using the second porous semiconductor peeling layer as an interface to obtain the first single crystalline semiconductor layer formed on the insulating layer.

B. Claims 1 and 84 Are Patentable

In the Final Office Action, claims 1 and 84 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Yonehara et al. (U.S. Patent No. 5,453,394). The Examiner has not made an adequate showing to support his rejections.

1. Yonehara et al. Fails to Disclose or Suggest Each Limitation of the Claims

Yonehara et al. is directed to a process for preparing a semiconductor substrate by bringing first and second substrates in contact. Yonehara et al. teaches that the viscosity characteristics at the bonding interface are changed by introducing an impurity to the region near the bonding interface, and that the microscopic unevenness at the bonding interface is reduced by the viscous movement of substances in the region near the bonding interface. (See col. 5,

lines 14-21). Thus, unbonded regions appearing at the bonding interface and the resulting voids are either reduced or eliminated by including a viscous flow-promoting layer at the bonding interface. (See col. 5, lines 21-25).

Yonehara et al. discloses three embodiments. (See col. 7, line 1, through col. 10, line 16). In the first embodiment depicted in Fig. 1, an insulating layer 102 is formed on the surface of a first substrate, and a viscous flow-promoting layer 103 is formed on the surface of the insulating layer. (See col. 7, lines 8-37). A second substrate 110 is then bonded to the first substrate 100 via the viscous flow-promoting layer 103. (See col. 7, lines 38-45 and Fig. 1).

In the second embodiment of Yonehara et al. depicted in Fig. 2, insulating layers 202 and 212 are provided on first and second substrates 200 and 210, respectively, and viscous flow-promoting layers 203 and 213 are provided on the surfaces of the insulating layers 202 and 212, respectively. (See col. 7, lines 49-55). The first and second substrates 200 and 210, respectively, are bonded together via the viscous flow-promoting layers 203 and 213, respectively. (See col. 7, lines 49-55 and Fig. 2). The first and second embodiments of Yonehara et al. simply illustrate that using a viscous flow-promoting layer at the bonding interface decreases or eliminates the voids at the bond. The substrates of both the first and second embodiments of Yonehara et al., depicted in Figs. 1 and 2, respectively, do not include a single crystalline semiconductor layer formed on the substrate via a porous semiconductor peeling layer, as required by the claims.

The Examiner appears to confuse the different layers disclosed in Yonehara et al. with the different layers in the claims. First, the Examiner refers to Fig. 2 in Yonehara et al. as disclosing the formation of two semiconductor layers on two porous substrates bonding the

substrates. Thus, the Examiner appears to relate the viscous flow-promoting layers 203 and 213 of Yonehara et al. to the semiconductor layers of the claims. The Examiner then refers to the epitaxial layer 302 in Fig. 3 of Yonehara et al. as one of the semiconductor layers of the claims. Thus, it is unclear what layers of Yonehara et al. the Examiner corresponds to the layers in the claims.

In the third embodiment of Yonehara et al. depicted in Figs. 3-7, a non-porous silicon layer 302 is grown on the porous silicon layer 301 of a first substrate 300. (See col. 7, line 59 through col. 8, line 49). The surface of the epitaxial layer 302 is oxidized to form an SiO_2 layer 303, and a silicon nitride film 303' is deposited on the SiO_2 layer 303. (See col. 8, lines 55-66). A heat softening insulator (viscous flow-promoting layer) 307 is then deposited on the surface of the oxide layer 303 or nitride layer 303'. (See col. 9, lines 9-11). The first substrate 300 and a second substrate 310 are then bonded to each other via the heat softening insulator 307. (See col. 9, lines 33-35 and Fig. 3E). In Yonehara et al., the first substrate 300 is removed by grinding, resulting in an exposed porous region 301 that is removed via etching. (See col. 9, lines 47-52). These steps result in a structure including the second substrate 310, the heat softening insulator 307, the silicon oxide film 303, and the epitaxial silicon layer 302. (See col. 10, lines 10-13 and Fig. 3F).

As discussed above, claims 1 and 84 each require two distinct separating steps: the first is the step of separating the seed substrate using the first porous semiconductor peeling layer as an interface; and the second is the step of separating the support substrate using the second porous semiconductor peeling layer as an interface. Yonehara et al. does not disclose two distinct separating steps toward producing a semiconductor device. Rather, Yonehara et al. only

describes removing the first substrate via grinding, and retaining the second substrate on the epitaxial silicon layer 302. (See Yonehara et al. at col. 9, lines 41-43; col. 10, lines 9-12; col. 12, lines 52-67; col. 13, lines 29-39; and col. 14, lines 3-13). Thus, Yonehara et al. does not disclose or suggest separating the support substrate using the second porous semiconductor peeling layer as an interface to obtain the first single crystalline semiconductor layer formed on the insulating layer, as required by the claims, and it would not have been obvious to one of ordinary skill in the art at the time of the invention to modify Yonehara et al. to derive claims 1 or 84. Although Appellant discussed this in the response after final, the Examiner failed to address this argument in his Advisory Action.

For the reasons set forth above, Appellant respectfully submits that claims 1 and 84 are allowable over Yonehara et al.

2. The Porosity and/or Thickness of the Porous Layer is Not Obvious

The Examiner also asserts that it would have been obvious to one of ordinary skill in the art at the time the invention was made to make the first porous layer have either a greater porosity (claim 1) or a greater thickness (claim 84) than the second layer. In support of this contention, the Examiner cites to *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980), and the rule that discovering an optimum value of a result effective variable involves only routine skill in the art. The Examiner further cites to Ohmi et al. (U.S. Patent Publication No. 2002/0093047) as disclosing that the porosity and the thickness of the porous layer effect the mechanical strength of the porous layer.

In the Final Office Action, the Examiner states that the layer with the greater porosity would separate more easily from the substrate. However, in Yonehara et al., the first

substrate 300 is removed by grinding, resulting in an exposed porous region 301 that is removed via etching. (See col. 9, lines 47-52). Thus, in Yonehara et al., the porosity and/or thickness of the porous layer does not affect the removal of the first substrate, which is removed via grinding. Moreover, according to Yonehara et al., it is actually desirable that the porous region at the separation interface be made thin, so that the etching time of the porous region is shortened. (See Yonehara et al. at col. 9, lines 61-65). Thus, Yonehara et al. teaches away from having a thicker porous layer.

For the reasons set forth above, Appellant respectfully submits that the claimed feature is not an optimum value of a result effective variable, as alleged by the Examiner.

C. Conclusion

Appellant respectfully submits that the subject matter of the claims on appeal is not disclosed or suggested by Yonehara et al. Thus, the Examiner has not made an adequate showing of obviousness with respect to the subject matter of the rejected claims. Appellant, therefore, respectfully requests reversal of the Examiner's decision to reject claims 1 and 84 under 35 U.S.C. § 103(a) as being unpatentable over Yonehara et al., and respectfully requests allowance of all pending claims.

Respectfully submitted,

Dated: June 20, 2006

By: _____

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VIII. CLAIMS APPENDIX

1. (Previously Presented) A method of production of an ultra-thin semiconductor device comprising the steps of:

forming a first single crystalline semiconductor layer on a seed substrate via a first porous semiconductor peeling layer;

bonding said seed substrate from said first single crystalline semiconductor layer side in the state with an insulating layer interposed to a support substrate having a second single crystalline semiconductor layer formed thereon via a second porous semiconductor peeling layer wherein the first porous semiconductor peeling layer has a greater porosity than the second porous semiconductor peeling layer;

separating said seed substrate using said first porous semiconductor peeling layer as an interface; and

separating said support substrate using said second porous semiconductor peeling layer as an interface to obtain said first single crystalline semiconductor layer formed on said insulating layer.

84. (Previously Presented) A method of production of an ultra-thin semiconductor device comprising the steps of:

forming a first single crystalline semiconductor layer on a seed substrate via a first porous semiconductor peeling layer;

bonding said seed substrate from said first single crystalline semiconductor layer side in the state with an insulating layer interposed to a support substrate having a second single crystalline semiconductor layer formed thereon via a second porous semiconductor peeling layer wherein the first porous semiconductor peeling layer has a greater thickness than the second porous semiconductor peeling layer;

separating said seed substrate using said first porous semiconductor peeling layer as an interface; and

separating said support substrate using said second porous semiconductor peeling layer as an interface to obtain said first single crystalline semiconductor layer formed on said insulating layer.

X. EVIDENCE APPENDIX

Appellant attaches hereto copies of the patents to (1) Yonehara et al. (U.S. Patent No. 5,453,394), which was relied upon by the Examiner in his rejection entered on December 20, 2005; and (2) Ohmi et al. (U.S. Patent Publication No. 2002/0093047), which was cited by the Examiner in his Advisory Action dated April 4, 2006.

US005453394A

United States Patent [19]

Yonehara et al.

[11] Patent Number: 5,453,394

[45] Date of Patent: Sep. 26, 1995

[54] **PROCESS FOR PREPARING SEMICONDUCTOR SUBSTRATE BY BRINGING FIRST AND SECOND SUBSTRATES IN CONTACT**

[75] Inventors: **Takao Yonehara**, Atsugi; **Kenji Yamagata**, Kawasaki, both of Japan

[73] Assignee: **Canon Kabushiki Kaisha**, Tokyo, Japan

[21] Appl. No.: **10,296**

[22] Filed: **Jan. 28, 1993**

[30] **Foreign Application Priority Data**

Jan. 31, 1992 [JP] Japan 4-46300

[51] **Int. Cl.**[6] **H01L 21/76**

[52] **U.S. Cl.** **437/62**; 437/974; 148/DIG. 12

[58] **Field of Search** ..... 148/DIG. 12, DIG. 135; 437/86, 966, 62, 914, 974

[56] **References Cited**

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472608	3/1992	Japan .

OTHER PUBLICATIONS

"A New Thinning Method for Obtaining Less than 100-nm-Thick Si Film on Wafer Bonding" by Kazuo Imai; Japanese Journal Of Applied Physics; vol. 30 No. 6 Jun. 1991; pp. 1154–1157.

"Single-Crystal Silicon On Non-Single-Crystal Insulators" by G. W. Cullen; Extended Abstracts; vol. 91–2, Oct. 13–17, 1991; pp. 674–749 Fall Meeting Of The Electrochemist Society.

Primary Examiner—George Fourson

Attorney, Agent, or Firm—Fitzpatrick, Cella, Harper & Scinto

[57] **ABSTRACT**

A process for preparing a semiconductor substrate comprises bringing a first substrate provided with at least one of boron and phosphorus on the surface of an insulating layer formed on the surface of the substrate in contact with a second substrate, and integrating both of the substrates by a heat treatment.

5 Claims, 7 Drawing Sheets

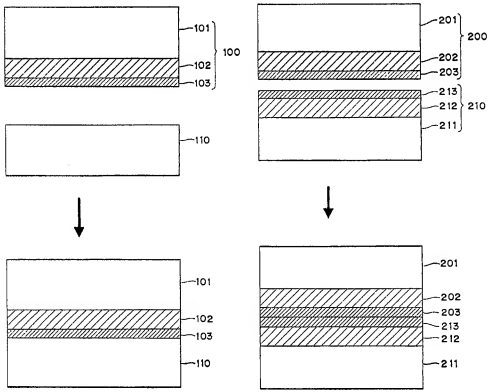


FIG. 1

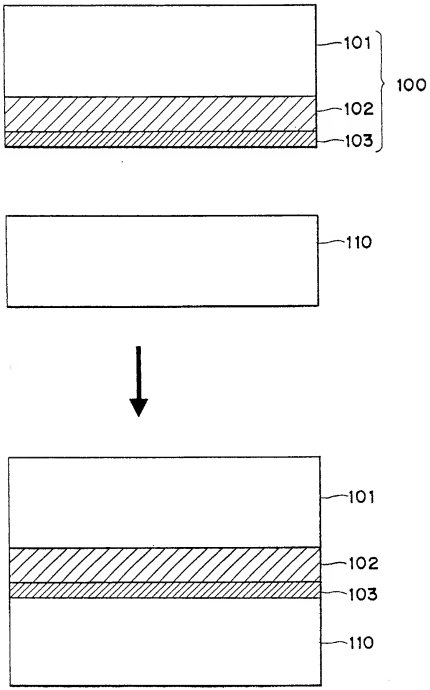


FIG. 2

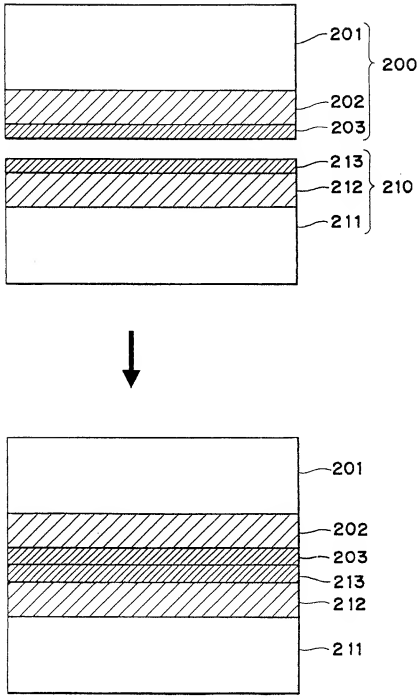


FIG. 3A

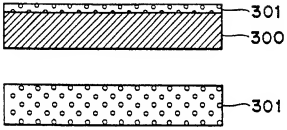


FIG. 3B

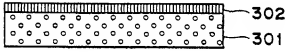


FIG. 3C

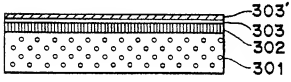


FIG. 3D

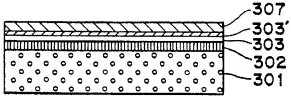


FIG. 3E

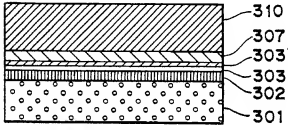


FIG. 3F

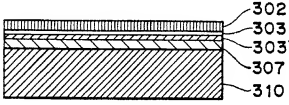


FIG. 4A

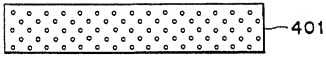


FIG. 4B

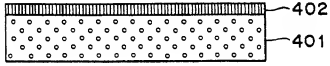


FIG. 4C

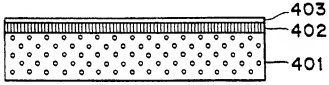


FIG. 4D

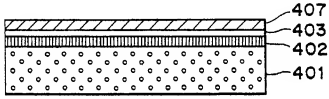


FIG. 4E

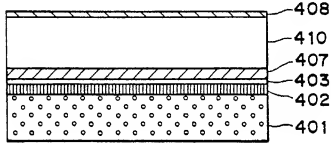


FIG. 4F

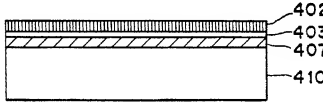


FIG. 5A

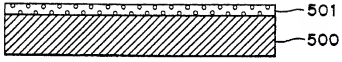


FIG. 5B

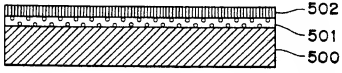


FIG. 5C

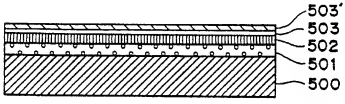


FIG. 5D

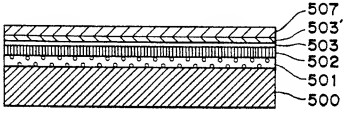


FIG. 5E

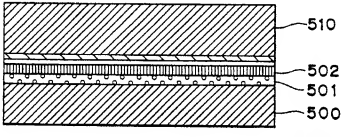


FIG. 5F

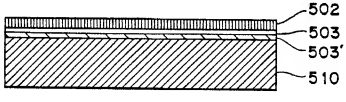


FIG. 6A

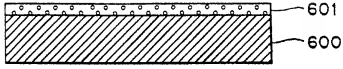


FIG. 6B

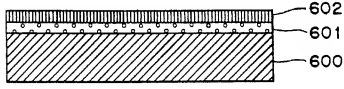


FIG. 6C

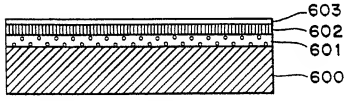


FIG. 6D

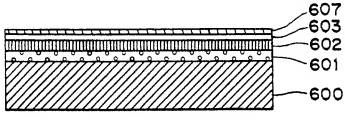


FIG. 6E

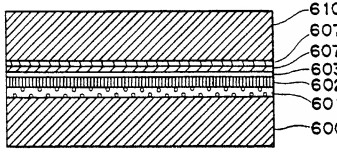


FIG. 6F

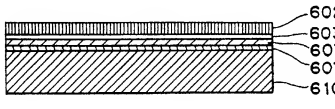


FIG. 7A

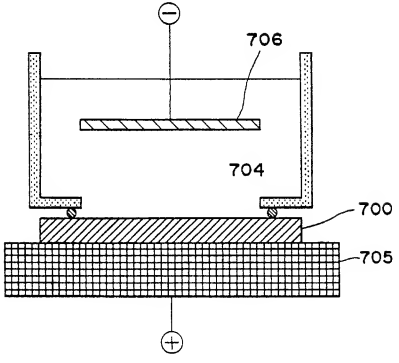
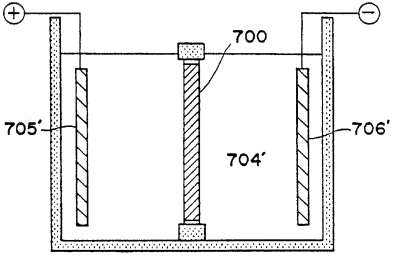


FIG. 7B



PROCESS FOR PREPARING SEMICONDUCTOR SUBSTRATE BY BRINGING FIRST AND SECOND SUBSTRATES IN CONTACT

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a semiconductor substrate and a process for the same, and more particularly to a semiconductor substrate by bonding and a process for preparing the same.

The present invention is suitably applied particularly to micromachine techniques, dielectric isolation techniques, SOI techniques, sensors, high power devices, communication high frequency band integrated circuit techniques, etc.

2. Related Background Art

Formation of a monocrystalline Si semiconductor layer on an insulator is widely known as a silicon-on-insulator (SOI) technique and has been extensively studied because devices based on utilization of the SOI technique have many advantages that have not been obtained in case of bulk Si substrates for preparing ordinary Si integrated circuits. That is, the following advantages can be obtained by utilizing the SOI technique:

1. Easy dielectric isolation with a possibility of higher level integration,
2. Distinguished resistance to radiation,
3. Reduced floating capacity with a possibility of higher speed,
4. Omission of well formation step,
5. Prevention of latch-up,
6. Possibility to form a fully deplated, field effect transistor by thin film formation, etc.

To obtain the above-mentioned many advantages of device characteristics, processes for forming the SOI structure have been studied for these more than ten years. The results are summarized, for example, in the following literature: Special Issue: "Single-crystal silicon on non-single-crystal insulators", edited by G. W. Cullen, Journal of Crystal Growth, Volume 63, No. 3, pp 429-590 (1983).

Among many SOI techniques, SOS (silicon-on-sapphire) formed by heteroepitaxial growth of a silicon film on a monocrystalline sapphire substrate by CVD (chemical vapor phase deposition) method disclosed in the past as a research example has advanced to such a level as to form practical integrated circuits, using monocrystal as a silicon layer and regarded as a successful, matured SOI technique. However, its wide application was interrupted by the occurrence of many crystal defects due to lattice mismatching at the interface between the Si layer and the underlayer sapphire substrate, by diffusion of aluminum into the Si layer from the sapphire substrate, and largely by a high cost of the substrate and delay in response to the formation of larger area.

Recently, some attempts have been made to form an SOI structure without using the sapphire substrate. The attempts can be classified into the following three major groups.

(1) After the surface oxidation of a silicon monocrystalline substrate, windows are made in a part of the oxide film to partially expose the silicon substrate, and a silicon monocrystalline layer is formed on the SiO_2 by epitaxial growth of silicon in the lateral direction, while utilizing the exposed silicon substrate as a seed.

(2) A silicon monocrystalline substrate itself is utilized as an active layer and an SiO_2 embedded layer is formed below by some means.

(3) After the silicon substrate is bonded to an insulating substrate, the silicon substrate is polished or ground or etched to leave the monocrystalline layer having a desired thickness.

Basically three processes are available as a means of realizing the above group (1): a process for direct epitaxial growth of a monocrystalline silicon layer in the lateral direction by CVD (gas phase process); a process for deposition of amorphous silicon and successive epitaxial growth in the lateral direction in the solid phase by heat treatment (solid phase process); and a process for irradiation of an amorphous or polycrystalline silicon layer with a converged energy beam such as an electron beam, a laser beam, etc. to make a monocrystalline silicon layer grow on SiO_2 through melting and recrystallization or scanning a melt zone by a rod heater bandwise (zone melting recrystallization) (liquid phase process).

These processes have advantages and disadvantages together, and still have many problems in the controllability, productivity, uniformity and quality, and thus have been hardly commercially used yet. For example, the CVD process requires grinding technique of good controllability or sacrificial oxidation to form a flat thin film, whereas the solid phase growth process suffers from poor crystallinity. The beam anneal process has problems in the treating time by scanning with the converged beam, the state of overlapped beams, focus adjustment, etc. Among them, the zone melting recrystallization process is the most matured process, by which relatively large integrated circuits have been made on trial, but there remain still many crystal defects such as quasigrain boundaries, etc. and thus minority carrier devices have not yet been made.

The technique now advanced by research and development by so many research organizations as a means of realizing the above group (2) is a process for forming a SiO_2 layer by oxgen ion implantation into a silicon monocrystalline substrate, called SIMOX (separation by ion implanted oxygen). This technique is now the most matured one because of good matching with the silicon process. However, in order to form the SiO_2 layer, oxygen ions must be implanted at least at 10^{18} ions/cm^2 and the implantation time is very long and the productivity is not so high. The wafer cost is also high. Furthermore, there remain many crystal defects. That is, no commercially satisfactory quality for making minority carrier devices can be obtained.

Besides SIMOX a process for forming SOI structure by dielectric isolation on the basis of oxidation of porous silicon is known. The process comprises forming an n-type silicon layer of island shape on the surface of a p-type silicon monocrystalline substrate by proton ion implantation (Imai et al: J. crystal Growth, Vol. 63, 547 (1983)) or by epitaxial growth and patterning, then making only the p-type silicon substrate porous by anodization in a HF solution so as to surround the silicon islands from the surface, and then dielectrically isolating the n-type silicon island by accelerated oxidation. This process has a problem that since the isolated silicon is determined before a device step the degree of freedom in a device design is limited.

As a means of realizing the above group (3), there is a technique of making the mirror surfaces of two wafers where an insulating film is formed on at least one of the mirror surfaces by oxidation, etc. to tightly adhere to each other, subjecting the wafers to a heat treatment to strengthen the bonding at the tightly adhered interface, and then grind-

ing or etching the bonded wafers from one side thereof thereby leaving a silicon monocrystalline thin film having a desired thickness on the insulating film. This technique is called "bonding SOI", and there are many problems to be solved in this technique. The most important problem is in a step of making the silicon substrate into a uniformly thin film. That is, a silicon substrate usually having a thickness of several hundred μm must be ground or etched uniformly to a thickness of several μm or less than 1 μm. This is technically very difficult from the viewpoint of controllability and uniformness. This technique has a possibility to provide a monocrystalline thin film of best quality in the SOI techniques, but has not been used in the commercial production because of the difficulty in the film thickness control.

Another important problem is a generation of a stress due to a difference in the coefficient of thermal expansion between two substrates, where an insulating substrate other than the silicon substrate is used as a support member. That is, there is substantially no problem when a silicon substrate is used as a support member (that is, bonding of two silicon substrates), but when other insulating substrate than silicon, for example, glass, is used as a support member, the substrates are sometimes warped, while keeping the bonding, or cracked or separated from each other due to a difference in the coefficient of thermal expansion in the heat treatment step at about 1,000° C. for strengthening the interface bonding after the two substrates are bonded together. There are cases of synthesizing materials having similar coefficients of thermal expansion to that of silicon and using them as a support substrate, but to our knowledge such synthetic materials have poor heat resistance and cannot endure the heat treatment for strengthening the bonding or the process temperature for forming devices.

Beside these problems, how to suppress the generation of voids (empty spaces formed at the bonding interface) is also a problem. There are many theories on the cause for generation of such voids. According to one theory, oxygen atoms or hydroxy groups covering the surfaces of bonded substrates mainly undergo dehydration and condensation to generate water vapors, and the generated water vapors get together to form voids. The thus generated voids can be made to disappear by further heat treatment at a higher temperature, thereby diffusing the vapors. Surface unevenness caused by dusts, scars etc. on the surface of the substrate will positively generate voids, and the voids generated by the surface unevenness of the substrate are very difficult to make to disappear.

As disclosed, for example, in the first international symposium on semiconductor wafer bonding science, technology, and applications, Extended Abstract of Fall meeting of Electrochemical Society, Phoenix, Ariz. Oct. 13–17, 1991, pp 674–749, the application of substrate bonding technique has been regarded as important in the field of not only SOI, but also micromachine structures, sensors, etc. and a substrate bonding technique capable of suppressing the generation of voids, and releasing the stresses generated at the bonding of substrates having different coefficients of thermal expansion, thereby preventing warpings has been keenly desired.

As described above, the technique capable of providing SOI substrates good enough to prepare electronic devices of improved characteristics with a high productivity has not been established yet.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a semiconductor substrate, where generation of fine voids due to the surface unevenness of bonded substrates is suppressed when an SOI substrate of high characteristics is prepared by bonding, and a process for preparing the same.

Another object of the present invention is a process for preparing a semiconductor substrate capable of releasing the stresses on a substrate when a silicon monocrystalline film is formed on the substrate having a different coefficient of thermal expansion from that of silicon.

A still another object of the present invention is to provide a process for preparing a semiconductor substrate which comprises bringing a first substrate provided with at least one of boron and phosphorus on the surface of an insulating layer formed on the surface of the substrate in contact with a second substrate, and heating the two substrates, thereby integrating the substrates.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1, 2, 3A–3F, 4A–4F, 5A–5F and 6A–6F are schematic views showing one example of the process for preparing a semiconductor substrate according to the present invention.

FIGS. 7A and 7B are schematic views showing one example of apparatuses for making a silicon substrate porous.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

According to a first aspect of the present invention, there is provided a process for preparing a semiconductor substrate which comprises bringing a first substrate provided with at least one of boron and phosphorus on the surface of an insulating layer formed on the surface of the substrate in contact with a second substrate, and heating the two substrates, thereby integrating the substrates.

According to a second aspect of the present invention, there is provided a process for preparing a semiconductor substrate which comprises bringing a first substrate and a second substrate each provided with at least one of boron and phosphorus on the surfaces of insulating layers formed on the surfaces of the substrates in contact with each other so that the insulating layers are in contact with each other, then heating the substrates, thereby integrating the substrates. According to a third aspect of the present invention, there is provided a process for preparing a semiconductor substrate which comprises a step of making an entire silicon monocrystalline substrate as a first substrate porous by anodization, a step of making a silicon monocrystalline thin film to epitaxially grow on one of the porous surfaces, a step of oxidizing the surface of the silicon monocrystalline thin film, a step of forming an insulating layer capable of softening by heat treatment on the oxidized surface, a step of making the insulating layer of the first substrate to tightly adhere to a second substrate, and a step of heat treating the first substrate and the second substrate tightly adhered to each other and then selectively etching the porous regions.

According to a fourth aspect of the present invention, there is provided a process for preparing a semiconductor substrate which comprises a step of making the surface layer on one side of a silicon monocrystalline substrate as a first substrate porous by anodization, a step of making a silicon monocrystalline thin film to epitaxially grow on the porous

surfacc, a step of oxidizing thc surface of the silicon monocrystalline thin film, a step of forming an insulating layer capable of softening by heat treatment on the oxidized surface, a step of making the insulating layer of the first substrate to tightly adhere to a second substrate, and a step of heat treating the first and second substrates tightly adhered to each other, then removing non-porous monocrystalline substrate regions of the first substrate, and then selectively etching the porous silicon regions.

According to a fifth aspect of the present invention, there is provided a semiconductor substrate prepared according to any one of the above-mentioned processes.

In the present process for preparing a semiconductor substrate, thc viscosity characteristics with respect to temperatures at the bonding interface are changed by introducing an impurity to the region near the bonding interface, and microscopic unevenness existing at the bonding interface is filled up by promoted viscous movement of substances in the region near the bonding interface, thereby making the unevenness to decreasc or disappear completely. That is, unbonded regions appearing at the bonding interface and the consequent voids, which are the most important problem in the wafer bonding technology, can be made to decrease or disappear completely for the first time.

Reflow of boron-phosphorus glass is known as one of the flattening procedures in the semiconductor integrated circuit production technique (R .A. Levy, K. Nassau: Solid State Technology, Japanese Edition, pp 69–71, November issue, 1986). Recently, Imai disclosed that voids can be reduced on the substrates having surface level differences by the presence of boron-phosphorus glass (Japanese Journal of Applied Physics, Vol. 30, No. 6, June, 1991, pp 1154–1157).

However, our extensive researches revealed that the surface of the glass deposited by chemical vapor deposition process, as disclosed in the above-mentioned report, had considerable unevenness and could not be used for bonding as such. Furthermore, the remaining of a large amount of boron and phosphorus, which serve as acceptors and donors, in the region near the bonding interface is a serious problem in the production of electronic devices, optical devices and micromachines.

In the present invention, an impurity capable of changing the viscosity of an insulating layer is imparted as a small amount of accelerated charged particles with a good controllability only to the surface of the thermally oxidized film maintaining a surface flatness of atomic level to form a viscous flow-promoting intermediate layer with a very high flatness, and the void-free bonding step as desired can be established for the first time.

When other materials than silicon, for example, quartz, is used as a second substrate serving as a support member, the entire substrates are considerably warped or the silicon film is peeled off or broken due to a difference in the coefficient of thermal expansion from the silicon substrate, and thus it is quite difficult to bond substrates of different materials to each other and subject the bonded substrates to heat treatment. However, when there is a viscous flow-promoting intermediate layer between the two materials and the intermediate layer is softened by heat treatment, the stresses generated between the different materials are released and warping, etc. of the substrates can be largely controlled. Thus, bonding of different materials to each other can be made possible.

A Preferable concentration of boron or phosphorus to be imparted to the surface of an insulating layer according to the present invention is not less than about 10% of B_2O_3 or not more than about 20% of P_2O_5 in SiO_2 in case of diffusion. By the addition at that concentration, the surface of the insulating layer can be softened within the process temperature (1100° C.). In casc of the presence of P_2O_5 or B_2O_3 at the above-mentioncd concentrations, softening starts at about 700° C.

When imparting of boron or phosphorus is carried out by ion implantation, a preferable amount of implanted ions is 1×10^{20} cm to 5×10^{21} cm^{-3}.

According to the present process for preparing a semiconductor substrate, a monocrystalline silicon layer is made to epitaxially grow on the porous surface of a silicon substrate, whose surface is partially or entirely made porous, and the epitaxially grown surface is oxidized. Then, a heat-softening insulating layer is formed on the oxidized surface to prepare a first substrate. The surface of the first substrate is heat treated to make the insulating layer to flow, thereby flattening the surface. Then, a second substrate serving as a support substrate is brought in tight contact with the first substrate. After the tight contact, the substrates are heat treated at a high temperature. Then, the porous silicon layer is selectively etched to obtain a silicon monocrystalline thin film (SOI) on the second substrate through the heat-softening insulating layer and the silicon oxide film. The silicon monocrystalline thin film is an epitaxial layer itself, and thus the film thickness can be highly controlled. On the oxidized surface of the epitaxial layer of the first substrate, unevenness, etc. due to the unevenness of the porous layer as the underlayer or due to the accelerated oxidation of crystal defects of epitaxial layer appear, and complete evenness is often not obtained. However, the heat-softening insulator deposited on the oxidized surface of the epitaxial layer effectively fills the unevenness at the interface and the flatness of the interface can be obtained by the flow of the heat-softening insulator.

In the practice of the present invention, the porous silicon has the following two important physical effects, one of which is an etching characteristic of porous silicon. Usually, silicon is hardly etched by hydrofluoric acid, but silicon made porous can be etched by hydrofluoric acid. Furthermore, with a liquid etching mixture of hydrofluoric acid, hydrogen peroxide and an alcohol, the porous silicon can be etched at a higher etching rate by about 10^{-5} or more than the non-porous silicon. Thus, a thin layer having a thickness of even about 1 μm can be selectively etched uniformly with a good controllability.

Another effect is an epitaxial growth characteristics. Porous silicon retains a monocrystalline structure as a crystal structure, and has pores having diameters of several tens to several hundreds Å extending from the surface inwards at a high density. An epitaxial layer growing on that surface can have a crystallinity equivalent to that of the epitaxial layer growing on a nonporous monocrystalline substrate. This is the characteristic. Thus, a monocrystalline thin film equivalent to the epitaxial layer growing on the monocrystalline silicon substrate of high reliability can be uscd as an active layer, and an SOI substrate having an excellent crystallinity, as compared with the conventional SOI substrate, can be provided in the present invention.

The present invention will be described in detail below, referring to the embodiments and the drawings.

Embodiment 1

In FIG. 1, a first substrate **100** and a second substrate **110** are composed of a single element semiconductor such as silicon, germanium, etc., a compound semiconductor such as gallium-arsenic, indium-phosphorus, etc., or glass such as transparent insulating quartz, etc.

At first, a flat insulating layer **102** is formed on the surface of the first substrate. In case that the first substrate is composed of silicon, the most suitable insulating layer **102** is a thermally oxidized film, and quantitative determination of the flatness by an interatomic force microscope reveals that a very flat surface having an unevenness of a few nanometers in the thickness direction is formed. However, as has been mentioned before, referring to the prior art, there are very fine unbonded regions at the bonding interface due to various causes, and it is very hard to obtain completely bonded interface characteristics. Main causes for incomplete bonding interface, or unbonded regions, occurrences of voids in the region near the interface seem to be local surface stainings, scars, level differences of crystal face, warping, etc., but have not been determined yet. When stable and thermally oxidized layer is not obtained at the interface like a compound semiconductor, the insulating layer is formed by chemical vapor deposition, particularly vacuum deposition or by sputtering.

Then, an impurity capable of promoting a viscous flow of the oxide is added to the surface of the insulating layer **102**, preferably down to about 100 nm maximum. In case the insulating layer is composed of silicon oxide, it is preferable to add boron or phosphorus thereto as an impurity. The addition can made by implantation of accelerated charged particles, that is, ion implanting, or by thermal decomposition, adsorption from a gas phase and deposition. In this manner, a viscous flow-promoting layer **103** can be formed on the surface of the insulating layer without deteriorating the flatness of the insulating layer.

The first substrate **100** and a second substrate **110** are carefully washed, dried and firmly bonded each other while heating the bonded substrates at least to a temperature where the viscosity of the viscous flow-promoting layer **103** is lowered. Though the flatness is very high, very fine voids due to the steps equivalent to the atomic surface can be made disappear by the viscous flow of the viscous flow-promoting layer.

Embodiment 2

According to an embodiment of the present invention shown in FIG. 2, insulating layers **202** and **212** are provided on a first substrate **200** and a second substrate **210**, respectively, and viscous flow-promoting layers **203** and **213** are also provided on the surfaces of the insulating layers **202** and **212**, respectively where even voids due to much larger surface unevenness can be made effectively to disappear.

Embodiment 3

Another embodiment of the present invention will be explained, referring to FIGS. 3A to 3F and 7A to 7B.

As shown in FIG. 3A, a monocrystalline silicon substrate **300** is anodized to form porous silicon **301**. The region to be made porous can be only a surface layer on one side of the substrate or can be extended to the entire substrate. In case of making the surface layer on one side porous, the region to be made porous can be extended to a thickness of 10 to 100 μm.

Procedure for forming porous silicon will be explained, referring to FIGS. 7A and 7B.

A p-type monocrystalline silicon substrate **700** is provided as a substrate and set in an apparatus shown in FIG. 7A. The substrate **700** may be of n-type, but must be limited to a substrate of low resistance in that case. One side of the substrate **700** is in contact with a hydrofluoric acid-based solution **704**, and a negative electrode **706** is provided on the solution side, and a positive metallic electrode **705** is in contact with the substrate **700** on the other side.

As shown in FIG. 7B, the positive electrode **705'** may be provided in the solution **704'** to apply a potential. In any way, the substrate **700** is made porous on the negative electrode side in contact with the hydrofluoric acid-based solution. As the hydrofluoric acid-based solution **704**, a concentrated hydrofluoric acid (49% HF) is usually used. When the concentrated hydrofluoric acid is gradually diluted with pure water (H_2O), etching will take place unpreferentially at some concentration, though dependent on a current density of an electric current to be passed. Since bubbles are generated on the surface of the substrate **700** during the anodization, an alcohol is added thereto as a surfactant in some cases to efficiently remove the bubbles. As an alcohol, methanol, ethanol, propanol, isopropanol, etc. can be used. In place of addition of the alcohol, anodizing can be carried out while stirring the solution with a stirrer.

The negative electrode **706** is composed of a material that is not corroded by the hydrofluoric acid-based solution, for example, gold (Au), platinum (Pt), etc. The positive electrode **705** can be composed of a metallic material in the ordinary use, and when the entire substrate **700** is anodized, the hydrofluoric acid-based solution **704** reaches the positive electrode **705**, and thus it is preferable to coat the surface of the positive electrode **705** with a hydrofluoric acid-resistant metallic film.

A current density for the anodizing is several hundreds mA/cm^2 at maximum, and its minimum may be any value except zero. The current density depends on a range capable of epitaxial growth of good quality on the surface of the porous silicon. The higher the current density, usually the higher the rate of anodization and the lower the density of the porous silicon layer, that is, the larger the volume occupied by the pores. That is, conditions for the epitaxial growth are changed thereby.

A non-porous monocrystalline silicon layer **302** is made to epitaxially grow on the thus formed porous silicon substrate or porous layer **301** (FIG. 3B). Epitaxial growth is carried out by ordinary thermal CVD, low pressure CVD, plasma CVD, molecular beam epitaxy, sputtering or the like. The thickness of the nonporous monocrystalline silicon layer thus formed must be equal to the design thickness of an SOI layer.

An SiO_2 layer **303** is formed by oxidizing the surface of the thus formed epitaxial layer **302** (FIG. 3C). The oxidation step has two meanings: one is an effect on a decrease in the interfacial level density of the epitaxial layer **302** as an active layer to the insulating underlayer interface when a device is formed on the finished SOI substrate, and another is an effect on suppression of diffusion from an impurity from an heat softening insulator (viscous flow-promoting layer) to be formed thereon in the next step. To further suppress the diffusion of the impurity to the epitaxial layer **302**, it is more effective to deposit a silicon nitride film **303'** on the epi-oxide film **303**. It is preferable for obtaining these two effects that the epi-oxide film has a thickness of 0.5 to

1.0 μm. When the epi-oxide film is used in combination with such a diffusion-preventing film as a silicon nitride film, etc., the thickness may be a little smaller. It is preferable that the silicon nitride film **303** has a thickness of 0.1 to 0.5 μm. When the thickness is smaller, the effect of the diffusion prevention will be lower, whereas when the thickness is larger, the silicon nitride film will be cracked due to internal stress of the film itself.

Then, a heat softening insulator (viscous flow-promoting layer) **307** is deposited on the surface of oxide layer **303** or nitride layer **303'** (FIG. 3D). The deposition is carried out usually by thermal CVD method, plasma CVD method or the like which comprises introducing an impurity gas such as PH_3, B_2H_6, etc. while decomposing an Si source gas such as Si_4, Si_2H_6, SiH_2Cl_2, etc. by oxidation. The thus obtained heat softening insulator **307** is an SiO_2 film containing a large amount of phosphorus (P) or boron (B) or these two, which are called PSG, BSG or BPSG, respectively. The higher the concentration of impurity in SiO_2, that is, phosphorus or boron concentration, the lower the softening start temperature of the SiO_2 film. The film thickness of heat softening insulator **307** can be selected, as desired, and is preferably about 0.1 μm to about 1.0 μm as a readily formable range by the ordinary process. In some cases the surface of the insulating film obtained by CVD has a considerable unevenness. The flatness of substrate is important in the bonding of substrates, it is preferable to heat treat the substrates so as to flatten the unevenness. Heat treatment temperature must be higher than the softening point (flowing temperature) of the deposited heat softening insulator **307**.

The first substrate is prepared by the foregoing steps.

Then, the first substrate and a second substrate **310** are bonded to each other at their mirror surfaces, and the bonded substrates are subjected to heat treatment (FIG. 3E). The heat treatment temperature is a flow temperature of the heat softening insulator deposited on the first substrate or higher. The second substrate **310** is not particularly limited and is selected from a silicon substrate, a quartz substrate or other ceramic substrates.

Then, the porous region **301** and others are selectively removed from the first substrate side, while leaving the epitaxial growth layer **302** (FIG. 3F). When the region to be removed extends the entire porous substrate **301**, the entire bonded substrates are dipped in a hydrofluoric acid-based solution, whereby the entire porous region **301** can be selectively etched. When the region to be etched contains a monocrystalline silicon substrate **300** as such, it is preferable to remove only the region of silicon substrate **300** by grinding, and when the porous region **301** is exposed, the grinding is completed and then the selective etching is carried out in the hydrofluoric acid-based solution. In any case, the monocrystalline epitaxial growth region **302** which is not porous, does not substantially undergo reaction with the hydrofluoric acid-based solution and thus remains as a thin film. When the second substrate **310** is composed mainly of SiO_2, it readily reacts with the hydrofluoric acid-based solution, and thus it is preferable to deposit a silicon nitride film or other substance hardly reactable with hydrofluoric acid on the opposite side to the bonding side by CVC, etc. in advance. When the porous region **301** is made thinner to some extent before dipping the substrates into the etching solution, the time required for the selective etching of the porous region can be shortened, and thus the second substrate can be prevented from unwanted reaction. When the second substrate is composed of Si which is not reactable with hydrofluoric acid, there are no such problems as above.

The hydrofluoric acid-based solution for the selective etching is a liquid mixture of hydrofluoric acid and hydrogen peroxide (H_2O_2) and/or an alcohol. Even a liquid mixture of hydrofluoric acid and nitric acid or further containing acetic acid can selectively etch the porous silicon, but the epitaxial silicon film **302** to be retained will be also etched to some extent in that case, and thus it is necessary to control the etching time, etc. exactly.

Through the foregoing steps, an SOI substrate comprising the second substrate **310**, the heat softening insulator **307**, the silicon oxide film **303** and the epitaxial silicon layer **302**, successived laid thereon, can be obtained.

The present invention will be explained in detail below, referring to the examples, but the present invention is not limited thereto.

EXAMPLE 1

A thermally oxidized film having a thickness of 0.5 μm was formed on the surface of a p-type (**100**) monocrystalline silicon substrate, 5 inches in diameter, and 0.1 to 0.2 Ω-cm in resistivity as a first substrate, and a viscous flow-promoting layer was formed in the surface layer to a depth of 0.1 μm from the surface of the thermally oxide film by ion implantation of boron and phosphorus onto the surface of the thermally oxidized film. The viscous flow-promoting layer contained 1×10^{20} atoms/cm^3 each of boron and phosphorus. Then, the first substrate was washed with a liquid mixture of hydrochloric acid, hydrogen peroxide and water and dried, and was tightly bonded to a monocrystalline silicon substrate as a second substrate, 5 inches in diameter, washed in the same manner as above, at room temperature. Then, the bonded substrates were heat treated in a nitrogen atmosphere at 1000° C. for 20 minutes. Observation of the bonded substrates by an X-ray topography revealed that there were no voids, and the tensile strength test showed that the bonding strength was 1000 kgf/cm^2 or higher.

The first substrate of the bonded substrates was ground and polished to a thin film having a thickness of 1 μm. When five voids (less than 10 μm in diameter) were detected with an optical microscope, no such voids were not found at all.

EXAMPLE 2

An epitaxial layer was formed on a p-type (**100**) silicon monocrystalline substrate having a resistivity of 0.01 Ω-cm as a first substrate to a thickness of 1.5 μm. The surface of the epitaxial layer was thermally oxidized to a depth of 0.5 μm in the same manner as in Example 1, and then 1×10^{21} atoms/cm^3 of phosphorus was ion-implanted into the surface region of the thermally oxidized layer to a depth of 0.1 μm.

As a second substrate, a silicon substrate provided with a thermally oxidizcd film having a thickness of 1 μm by thermally oxidation and a boron-implanted surface region containing 1×10^{20} atoms/cm^3 of boron on the surface of the thermally oxided film is formed. Both substrates were washed with a liquid mixture of hydrochloric acid, hydrogen peroxide and water, dried and tightly bonded to each other at room temperature. Then, the bonded substrate was heat treated in a nitrogen atmosphere at 1100° C. for 60 minutes.

Observation of the bonded substrates revealed that there were no voids, and the tensile strength test revealed that the bonding strength was 1200 kgf/cm^2 or higher.

EXAMPLE 3

An epitaxial layer was formed on a p-type (100) silicon monocrystalline substrate having a resistivity of 0.01 Ω-cm as a first substrate to a thickness of 1.5 μm. The surface of the epitaxial layer was thermally oxidized to a depth of 0.5 μm, and then 1×10^{21} atoms/cm^3 each of boron and phosphorus was ion-implanted into the surface region of the thermally oxidized layer to a depth of 0.1 μm.

As a second substrate, a fused quartz substrate ion-implanted with 1×10^{20} atoms/cm^3 each of boron and phosphorus into the surface region to a depth of 0.1 μm and then both substrates were washed with a liquid mixture of hydrochloric acid, hydrogen peroxide and water, dried and tightly bonded to each other at room temperature. Then, the bonded substrate was heat treated in a nitrogen atmosphere at 200° C. for 6 hours.

Observation of the bonded substrates revealed that there were no voids, and the tensile strength test revealed that the bonding strength was 500 kgf/cm^2 or higher.

EXAMPLE 4

The fourth example of the present invention will be explained in detail, referring to FIGS. 3A to 3F and 7A to 7B.

A p-type (100) monocrystalline silicon substrate having a thickness of 200 μm, a resistivity of 0.1 to 0.2 Ω-cm and a diameter of 4 inches was set in an apparatus as shown in FIG. 7A and subjected to anodization to obtain porous silicon **301** (FIG. 3A).

As a solution **704**, 49% HF solution was used at a current density of 100 mA/cm^2. The rate of making the substrate porous was 8.4 μm/min. and the p-type (100) silicon substrate having a thickness of 200 μm was entirely made porous within 24 minutes.

A monocrystalline silicon layer **302** was made to epitaxially grow on the p-type (100) porous silicon substrate **301** to a thickness of 1.0 μm by CVD method under the following deposition conditions (FIG. 3B).

Source gas: SiH_4/H_2

Gas flow rate: 0.62/140 (liter/min.)

Temperature: 750° C.

Pressure: 80 Torr

Growth rate: 0.12 μm/min.

The surface of the expitaxial growth layer **302** was oxidized in a steam atmosphere at 1000° C. to obtain as SiO_2 **303** film having a thickness of 0.5 μm (FIG. 3C).

A BPSG film **307** was deposited on the oxide film **303** to a thickness of 0.7 μm by thermal CVD, using a gas mixture of SiH_4, O_2, PH_3 (diluted with N_2), and B_2H_6(diluted with N_2) (FIG. 3D). Furthermore, to flatten fine unevenness on the surface of the BPSG film, the substrate was heat treated in an oxygen atmosphere at 1000° C. for 30 minutes. The substrate prepared in this manner was used as a first substrate.

The first substrate and another silicon substrate **310** as a second substrate were washed with a solution of HCl, H_2O_2 and H_2O, and then thoroughly washed with water. Then, the first substrate and the second substrate were bonded to each other at the mirror surfaces and the bonded substrates were heat treated in a nitrogen atmosphere at 1100° C. for 2 hours to increase the bonding force at the interface between the bonded substrates (FIG. 3E).

After the heat treatment, the tightly bonded substrates were dipped in a selective etching solution to selectively etch only the porous portion **301** (FIG. 3F). Composition of the etching solution and the etching rate of porous silicon are as follows:

$HF:H_2O_2:C_2H_5OH$=5:25:6, and

Etching rate:1.6 μm/min.

The porous portion having a thickness of 200 μm was entirely etched within about 125 minutes, where the etching rate of monocrystalline silicon layer **302** was 0.0006 μm/hour and the monocrystalline silicon layer **302** remained without substantial etching.

Through the foregoing steps, an SOI substrate comprising the BPSG film **307**, the silicon oxide film **303** and the epitaxial layer **302** successively formed on the silicon substrate **310**, was obtained.

EXAMPLE 5

The fifth example of the present invention will be explained in detail, referring to FIGS. 4A to 4F.

A p-type (100) silicon substrate **400** having a thickness of 400 μm and a resistivity of 0.01 Ω-cm was made entirely porous to form a porous substrate **401** in the same manner as in Example 4 (FIG. 4A).

Then, an epitaxial layer **402** was formed on one surface of the substrate to a thickness of 0.5 μm in the same manner as in Example 4 (FIG. 4B), and an oxide film **403** having a thickness of 0.5 μm was formed on the surface of the epitaxial layer **402** (FIG. 4C). By the oxidation, the thickness of the epitaxial layer **402** was reduced to about 0.25 μm.

Then, a BPSG film **407** was deposited on the thus formed oxide film **403** in the same manner as in Example 4 (FIG. 4D), and the flattening of the surface of the BPSG film **407** was carried out in the same manner as in Example 4 to prepare a first substrate.

The first substrate and another fused quartz substrate **410**, 4 inches in diameter, were washed and bonded to each other at the mirror surfaces, and the bonded substrates were heat treated at 500° C. for 30 minutes. After the heat treatment, a silicon nitride film **408** was deposited on the outer surface of the quartz substrate **410** to a thickness of 0.3 μm by plasma CVD as a protective film for the successive selective etching step. The nitride film **408** had a silicon-rich composition, compared with the ordinary composition, i.e. Si:N= 3.7:4, to increase the resistance to etching by hydrofluoric acid (FIG. 4E).

Then, the porous silicon portion **401** was selectively etched away in the same etching procedure as in Example 4. The silicon nitride film **408** as the protective film disappeared almost at the same time when the porous silicon substrate **401** was entirely etched away, while the quartz substrate **410** was etched only to a depth of a few μm (FIG. 4F).

Finally, the entire substrate was heat treated at 1100° C., which was higher than the flow temperature of BPSG, for one hour to increase the bonding strength at the bonding interface.

Through the foregoing steps, an SOI substrate comprising the BPSG film **407**, the silicon oxide film **403** and the epitaxial film **402** successively formed on the quartz substrate **410** was obtained.

EXAMPLE 6

The sixth example of the present invention will be explained in detail, referring to FIGS. 5A to 5F.

A p-type (100) silicon substrate **500** having a thickness of 400 μm and a resistivity of 0.01 Ω·cm was made to porous only to a depth of 20 μm from the surface to form a porous layer **501** (FIG. 5A).

An epitaxial layer **502** was formed on the porous surface of the substrate to a thickness of 0.5 μm in the same manner as in Example 4 (FIG. 5B).

An oxide film **503** was formed on the surface of the epitaxial layer **502** to a thickness of 0.5 μm (FIG. 5C). By the oxidation, the thickness of the epitaxial layer **502** was reduced to about 0.25 μm. Then, a silicon nitride film **503'** was deposited on the surface of the oxide film **502** to a thickness of 0.2 μm by LPCVD. A BPSG film **507** was deposited on the surface of the silicon nitride film **503'** to a thickness of 0.5 μm by plasma CVD (FIG. 5D). Fine unevenness on the BPSG surface was flattened by the same flow procedure as in Example 4, whereby a first substrate was obtained.

The first substrate and another silicon substrate **510**, 4 inches in diameter, as a second substrate, were washed and then bonded to each other at the mirror surfaces, and the bonded substrates were heat treated at 1100° C. for 2 hours (FIG. 5E).

The monocrystalline silicon substrate portion **500** of the first substrate was entirely ground by mechanical grinding to expose the porous portion **501**, and then the porous silicon portion **501** was selectively etched in the same manner as in Example 4. The thickness of the porous silicon portion to be etched **501** was only about 20 μm, and thus the porous silicon portion **501** was entirely etched away within about 10 minutes, whereby an SOI substrate comprising the BPSG film **507**, the silicon nitride film **503'** the silicon oxide film **503** and the epitaxial layer **502** successively formed on the silicon substrate **510** was obtained (FIG. 5F).

EXAMPLE 7

The seventh example of the present invention will be explained in detail, referring to FIGS. 6A to 6F.

A p-type (100) silicon substrate **600** having a thickness of 400 μm and a resistivity of 0.01 Ω·cm was made porous only to a depth 20 μm from the surface to form a porous layer **601** (FIG. 6A).

An epitaxial layer **602** was formed on the porous surface of the substrate to a thickness of 0.5 μm in the same manner as in Example 4 (FIG. 6B). Then the surface of the epitaxial layer **602** was oxidized in steam at 1000° C. to form an oxide film **603** having a thickness of 0.5 μm. Consequently, the thickness of the silicon monocrystalline portion **602** of the epitaxial layer was reduced to 0.25 μm (FIG. 6C).

Then, a BPSG film **607** was deposited on the surface of the oxide film **603** to a thickness of 0.2 μm by plasma CVD, and flattening by surface flow by heat treatment was carried out (FIG. 6D) to obtain a first substrate.

Another silicon substrate **610**, 4 inches in diameter, as a second substrate was provided with a BPSG film **607'** on the surface of substrate **610** to a thickness of 0.2 μm by plasma CVD, and the surface of the BPSG film **607'** was flattened also by the surface flow. Then, the first substrate and the seeond substrate were bonded to each other at the BPSG surfaces, and then the bonded substrates were heat treated at 1100° C. for 2 hours (FIG. 6E).

The entire monocrystalline silicon substrate portion **600** of the first substrate was ground by mechanical grinding to expose the porous portion **601**. Then, the porous silicon portion **601** was selectively etched in the same etching procedure as in Example 4. The thickness of the porous silicon portion **601** to be etched was only about 20 μm, and thus the entire porous silicon portion **601** was etched away within about 10 minutes, whereby an SOI substrate comprising the BPSG films **607** and **607'**, the silicon oxide film **603** and the epitaxial layer **602** successively formed on the silicon substrate **610** was obtained (FIG. 6F).

As described in detail above, bonded substrates with a good bonding interface without voids can be obtained by providing a viscous flow-promoting intermediate layer in the region near the interface according to the present invention, and can be used in various applications.

According to the present process for preparing a bonded SOI substrate which comprises the steps of successively forming a monocrystalline epitaxial growth layer, an oxidized layer thereof, and a heat softening insulating layer on porous silicon to prepare a first substrate bonding the first substrate to a second substrate, heat treating the bonded substrates and seleetively removing the porous silicon, since generation of voids (unbonded parts) due to fine surface unevenness can be prevented and stresses on the substrates generated at the bonding interface by heat treatment can be released, an SOI substrate free from warping can be provided.

What is claimed is:

1. A process for preparing a semiconductor substrate comprising:

providing a first substrate having a semiconductor layer and an insulating layer;

forming a first layer comprising an element constituting said insulating layer and at least one of boron and phosphorus on the surface of said insulating layer;

contacting the first layer with a second substrate; and

integrating both of the substrates by a heat treatment to form the semiconductor substrate,

wherein the boron and/or the phosphorus are provided on the surface of the insulating layer by ion implantation.

2. A process for preparing a semiconductor substrate which comprises bringing a first substrate and a second substrate each provided with at least one of boron and phosphorus on the surface of an insulating layer on the surface of the substrate in contact with each other so that the insulating layers are in contact with each other, and integrating both of the substrates by a heat treatment, wherein the boron and/or the phosphorus are provided on the surface of the insulating layer by ion implantation.

3. A process according to claims **1** or **2**, wherein the first substrate and the second substrate are single element semiconductors, compound semiconductors or one of the first and second substrates is glass.

4. A process according to claim 1, wherein the thickness of said first layer is in a range of from 0.1 to 1.0 μm.

5. A process according to claim 1 or **2**, wherein the boron and/or the phosphorus are ion implanted in an amount ranging from 1×10^{20} to 5×10^{21} cm^{-3}.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 5,453,394

DATED : September 26, 1995

INVENTOR(S) : TAKAO YONEHARA ET AL.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On Title page;

AT [56] REFERENCES CITED

Foreign Patent Documents,

"1189145 7/1989 Japan
3173422 7/1991 Japan
472608 3/1992 Japan" should read
--1-189145 7/1989 Japan
3-173422 7/1991 Japan
4-72608 3/1992 Japan--.

COLUMN 3

Line 23 "other" should read --another--.
Line 54 "Phoenis," should read --Phoenix,--

COLUMN 4

Line 48 "According" should read --¶ According--.

COLUMN 5

Line 34 "researches" should read --research--.
Line 51 "is" should read --are--.
Line 65 "Preferable" should read --preferable--.

COLUMN 6

Line 11 "1x10^{20}cm" should read --1x10^{20}cm^{-3}--.
Line 51 "characteristics." should read
--characteristic.--.

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 5,453,394

DATED : September 26, 1995

INVENTOR(S) : TAKEO YONEHARA ET AL.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

COLUMN 7

Line 32 "can" should read --can be--.
Line 39 "bonded" should read --bonded to--.
Line 43 "made" should read --made to--.

COLUMN 8

Line 19 "unprefeventially" should read --unpreferentially--.
Line 62 "an" should read --a--.

COLUMN 9

Line 24 "In" should read --¶ In--.

COLUM 10

Line 12 "successived" should read --successively--.
Line 26 "oxide" should read --oxidized--.
Line 57 "thermally" should read --thermal--.
Line 59 "oxided" should read --oxidized--.

COLUMN 11

Line 48 "as" should read --an--.

COLUMN 13

Line 5 "to" should be deleted.

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 5,453,394

DATED : September 26, 1995

INVENTOR(S) : TAKAO YONEHARA ET AL.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

COLUMN 14

Line 54 "claims" should read --claim--.

Signed and Sealed this

Fourteenth Day of May, 1996

Attest:

BRUCE LEHMAN

Attesting Officer *Commissioner of Patents and Trademarks*

US 20020093047A1

(19) United States

(12) Patent Application Publication (10) Pub. No.: US 2002/0093047 A1

Ohmi et al. (43) Pub. Date: Jul. 18, 2002

(54) COMPOSITE MEMBER, ITS SEPARATION METHOD, AND PREPARATION METHOD OF SEMICONDUCTOR SUBSTRATE BY UTILIZATION THEREOF

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Correspondence Address:
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NEW YORK, NY 10112 (US)

(21) Appl. No.: 10/020,807

(22) Filed: Dec. 18, 2001

Related U.S. Application Data

(62) Division of application No. 09/250,242, filed on Feb. 16, 1999, now Pat. No. 6,342,433.

(30) Foreign Application Priority Data

Feb. 18, 1998 (JP) 10-035820

Publication Classification

(51) Int. Cl.[7] H01L 29/792

(52) U.S. Cl. 257/324

(57) ABSTRACT

In order to separate first and second base substrate without cracking them, and use a damaged base substrate again as a semiconductor substrate to enhance a yield, there is disclosed a preparation method of a semiconductor substrate comprising the steps of separating a composite member formed by bonding the first and second base substrates to each other via an insulating layer into a plurality of members at a separation area formed in a position different from a bonded face to transfer a part of one base substrate onto the other base. A mechanical strength of the separation area is non-uniform along the bonded face in the composite member.

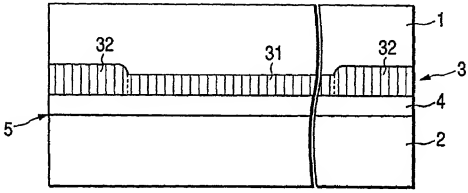


FIG. 1A

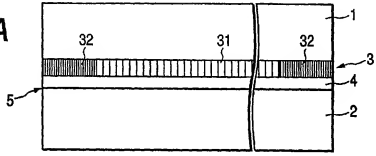


FIG. 1B

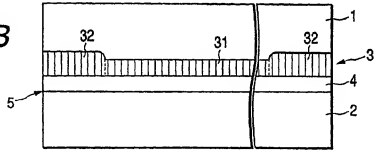


FIG. 1C

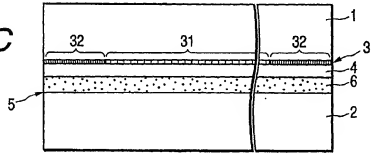


FIG. 2A

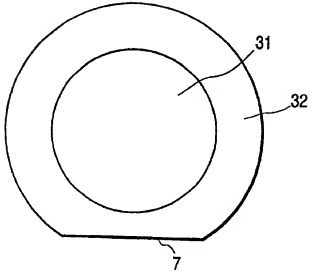


FIG. 2B

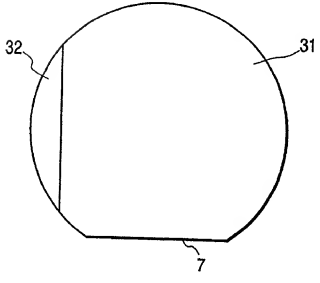


FIG. 3A

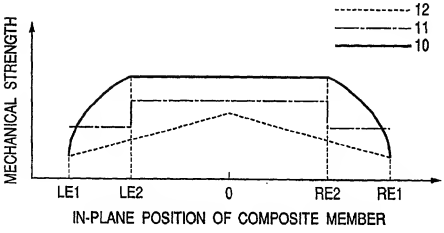

12
11
10
MECHANICAL STRENGTH
LE1
LE2
0
RE2
RE1
IN-PLANE POSITION OF COMPOSITE MEMBER

FIG. 3B

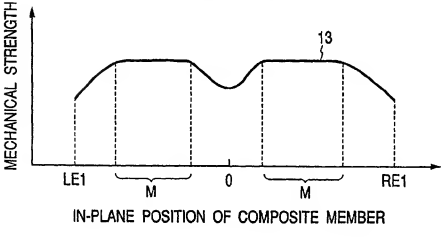

13
MECHANICAL STRENGTH
LE1
M
0
M
RE1
IN-PLANE POSITION OF COMPOSITE MEMBER

FIG. 4

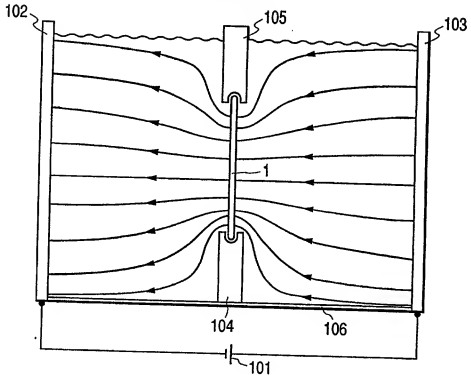

102
105
103
1
104
106
101

FIG. 5

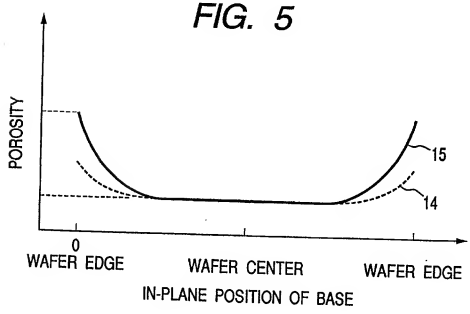

POROSITY
15
14
0
WAFER EDGE
WAFER CENTER
WAFER EDGE
IN-PLANE POSITION OF BASE

FIG. 6A

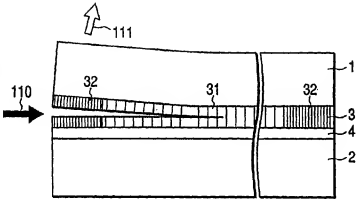


FIG. 6B

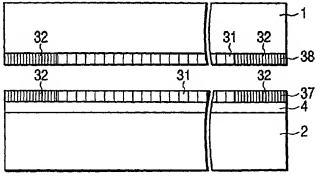


FIG. 6C

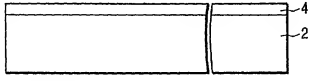


FIG. 7

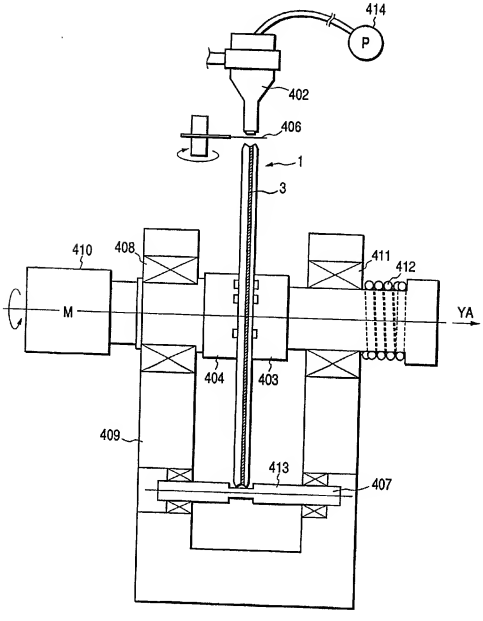


FIG. 8

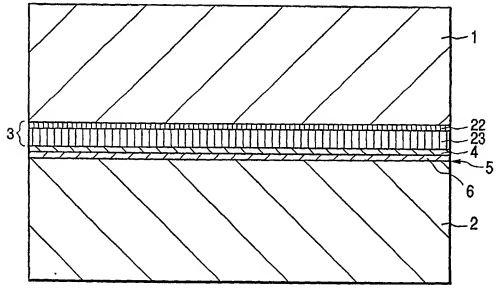


FIG. 9

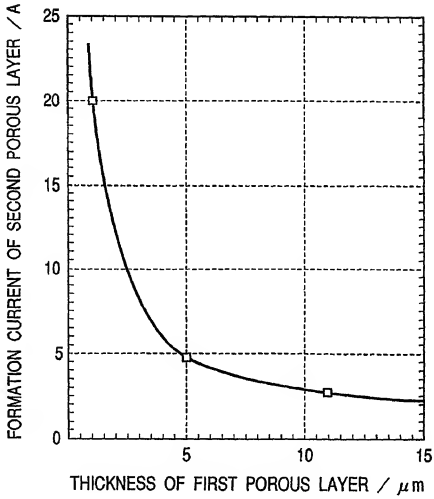

FORMATION CURRENT OF SECOND POROUS LAYER / A
25
20
15
10
5
0
5
10
15
THICKNESS OF FIRST POROUS LAYER / μm

FIG. 10

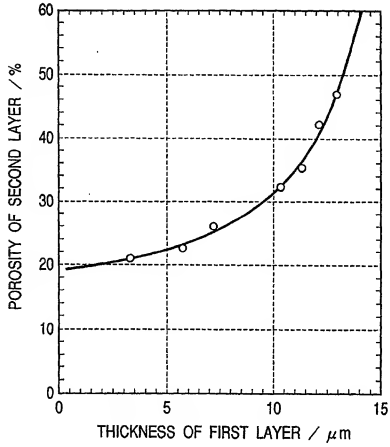

60
50
40
30
20
10
0
POROSITY OF SECOND LAYER / %
0
5
10
15
THICKNESS OF FIRST LAYER / μm

FIG. 11

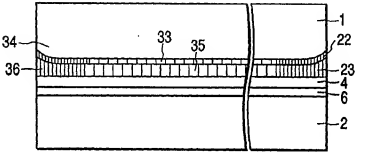


FIG. 12A

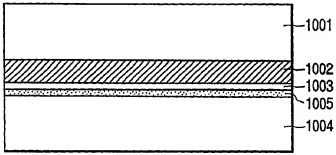


FIG. 12B

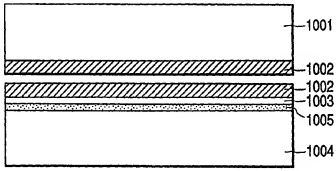
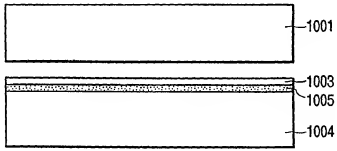


FIG. 12C



COMPOSITE MEMBER, ITS SEPARATION METHOD, AND PREPARATION METHOD OF SEMICONDUCTOR SUBSTRATE BY UTILIZATION THEREOF

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to a composite member, its separation method and a preparation method of a semiconductor substrate, particularly to a composite member having inside a fragile structure with a low mechanical strength, its separation method and a preparation method of a semiconductor substrate. The present invention is particularly suitable for a preparation method of a substrate (SOI substrate) having an SOI (semiconductor on insulator) structure as a type of semiconductor substrate.

[0003] 2. Related Background Art

[0004] A device using the SOI substrate has various advantages which cannot be attained by an ordinary Si substrate. For example, the advantages are as follows:

[0005] (1) a dielectric is easily separated, and the device is suitable for high integration;

[0006] (2) the device is superior in resistance to rays;

[0007] (3) a floating capacity is small, and high speed operation of elements is realized;

[0008] (4) a well process is unnecessary;

[0009] (5) latch-up can be prevented; and

[0010] (6) a complete depletion type field-effect transistor can be formed by thinning films.

[0011] Since the SOI structure has various advantages as described above, researches concerning its forming method have been advanced these several decades. Known as a conventional SOI technique is an SOS (silicon on sapphire) technique for forming Si on a single-crystal sapphire substrate by hetero epitaxial growth in CVD (chemical vapor deposition) method. The SOS technique has been evaluated as most matured SOI technique, but has not been put to practical use because of a large amount of crystal defects caused by lattice mismatching in an interface of an SI layer and a base sapphire substrate, mixture of aluminum constituting the sapphire substrate into the Si layer, substrate price, delay in area enlargement, and for other reasons.

[0012] Following the SOS technique, an SIMOX (separation by ion implanted oxygen) technique has appeared. Concerning the SIMOX technique, various methods have been developed aiming at reduction of the crystal defects or reduction of manufacture cost. Examples of the methods include a method of injecting oxygen ions to a substrate to form an embedded oxide layer; a method of bonding two wafers via an oxide film, polishing or etching one of the wafers, and leaving a thin single-crystal Si layer on the oxide film; a method of implanting hydrogen ions into a predetermined depth from a surface of an Si substrate with an oxide film formed thereon, bonding with the other substrate, leaving a thin single-crystal Si layer on the oxide film by heating or another treatment, and peeling off the bonded substrate (other substrate); and the like.

[0013] A new SOI technique has been disclosed in Japanese Patent No. 2,608,351 or U.S. Pat. No. 5,371,037. In the technique, a first substrate obtained by forming a non-porous single-crystal layer on a single-crystal semiconductor substrate with a porous layer formed thereon is bonded on a second substrate and these substrates are bonded, then unnecessary portions are removed, so that the nonporous single-crystal layer is transferred to the second substrate. The technique is superior in that the SOI layer has a superior film thickness uniformity, a crystal defect density of the SOI layer can be reduced, the SOI layer has a good surface flatness, a manufacture device with expensive and special specifications is unnecessary and that SOI substrates having SOI films in the range of about several 10 nm to 10 μm can be manufactured with the same manufacture device.

[0014] Furthermore, the present applicant has disclosed a technique in Japanese Patent Application Laid-open No. 7-302889, in which after first and second substrates are bonded, the first substrate is separated from the second substrate without being collapsed, a surface of the separated first substrate is then smoothed, and a porous layer is formed thereon again, so that the first substrate is reused. An example of the proposed method will be described with reference to **FIGS. 12A** to **12C**. After a surface layer of a first Si substrate **1001** is made porous to form a porous layer **1002**, a single-crystal Si layer **1003** is formed on the layer **1002**, and the single-crystal Si layer and a main surface of a second Si substrate **1004** separate from a first Si base substrate are bonded to each other via an insulating layer **1005** (**FIG. 12A**). Thereafter, a wafer bonded via the porous layer is divided (**FIG. 12B**), and the porous Si layer exposed to the surface of a second Si base substrate is selectively removed to form an SOI substrate (**FIG. 12C**). The first Si substrate **1001** can be reused by removing the remaining porous layer therefrom.

[0015] In the invention disclosed in Japanese Patent Application Laid-open No. 7-302889, the substrate is separated using the property that the structure of the porous silicon layer is more fragile than a non-porous silicon. Since the substrate once used in preparation of the semiconductor substrate can be used again in preparation of the semiconductor substrate, the cost of the semiconductor substrate can effectively be reduced. Moreover, in the technique, since the first substrate can be used without being wasted, the manufacture cost can largely be reduced. Additionally, the manufacture process is advantageously simple.

[0016] Examples of the method for separating the first and second base substrates (base plates) include pressurizing, pulling, shearing, wedge insertion, thermal treatment, oxidization, vibration application, wire cutting, and the like. Additionally, the present inventors have proposed a separation method in Japanese Patent Application No. 9-75498 or U.S. patent application No. 047,327 filed on Mar. 25, 1998, in which fluid is sprayed to a separation area. Gas and/or liquid is used as the fluid, and especially a water jet using a liquid mainly composed of water is preferable. In the method, at the time of separating, water not only cuts a bonded face but also uniformly enters a gap between the first and second bases, so that a relatively uniform separating pressure can be applied to the entire separation face. Moreover, in the method, different from the case where gas is not used, particles can be washed away without being scattered. The method is superior in these two respects to the separa-

tion method by the wedge insertion. Especially, when the mechanical strength of the separation area is set lower than that of the bonded place, only the fragile portion is ruptured, collapsed or removed by spraying the fluid flow to the separation area, and another strong portion can advantageously be left without being collapsed.

[0017] However, when the water jet or another fluid is used to separate the bonded composite member by spraying the fluid to a side face of a composite member, especially around a side face of the separation area, there is a case where the fluid flow cannot easily break or cut the separation area because the separation area has an excessive strength. In this case, the composite member can be separated by raising a fluid pressure, but if the pressure is excessively raised, cracks advance inward from the side face of the bonded base. In the midst, one or both of the separated base substrates may be cracked by the pressure of the fluid injected to the separation area. Therefore, yield is lowered in the separating process. To avoid this, there is provided a method of further lowering the mechanical strength of the separation area to form a more fragile structure. If the structure is excessively fragile, however, a problem is caused that the separation area is broken and cannot be bonded or that the separation area is broken to generate particles as contaminants during heating, cleaning, or handling the base substrate otherwise in a process of preparing the composite member.

[0018] Moreover, when separation is performed in another method without using the fluid, basically the similar problem is caused. Therefore, the yield in the separating process may be lowered.

SUMMARY OF THE INVENTION

[0019] An object of the present invention is to provide a composite member and its separation method in which the composite member can be separated relatively easily without damaging separated bases.

[0020] Another object of the present invention is to provide a composite member and its separation method in which a mechanical strength of a major separation area can be relatively raised, unintended collapse of the separation area is prevented, and generation of particles is suppressed.

[0021] According to an aspect of the present invention, there is provided a preparation method of a semiconductor substrate using a separation method of a composite member comprising the step of separating the composite member into a plurality of members at a separation area, in which a mechanical strength of the separation area is non-uniform along a bonded face.

[0022] Especially, in the separation area, a peripheral portion of the composite member is preferably lower in mechanical strength than a central portion. Additionally, the separation area is preferably lower in mechanical strength than the bonded interface.

[0023] According to another aspect of the present invention, there is provided a preparation method of a semiconductor substrate using the separation method mentioned above.

[0024] According to still another aspect of the present invention, there is provided a preparation method of a semiconductor substrate which comprises separating a composite member formed by bonding a first base substrate and a second base substrate to each other into a plurality of members at a separation area formed in a position different from a bonded face, a mechanical strength of the separation area being non-uniform along the bonded face, and a mechanical strength of a peripheral portion of the separation area being locally low.

[0025] According to a further aspect of the present invention, there is provided a composite member comprising a separation area inside, a mechanical strength of the separation area being non-uniform along a surface of the composite member, a mechanical strength of a peripheral portion of the separation area being locally low.

[0026] For the separation area, a porous layer formed by anodization, a layer formed by implanting ions in which microcavities can be obtained, or the like can be used. When an Si wafer or another semiconductor substrate, or a quartz wafer is used as a first or second base, it substantially has a disc shape although it has an orientation flat or a notch. Therefore, the composite member obtained by bonding the first and second base substrates to each other also has a substantially disc shape. In this case, when the mechanical strength of the separation area is non-uniform in such a manner that the strength is high in the central portion of the composite member and low in its peripheral portion, and substantially uniform in a circumferential direction, the composite member can effectively be separated. When the composite member is a rectangular plate member, the mechanical strength of its corner, side or entire periphery is lowered.

[0027] The mechanical strength can be made non-uniform by forming portions different in porosity from one another in the separation area. As the porosity is increased, the mechanical strength is lowered. Therefore, the mechanical strength can be changed by changing the porosity. Specifically, the mechanical strength of the peripheral portion can be lowered by setting higher the porosity in the peripheral portion than in the central portion.

[0028] The mechanical strength can also be made non-uniform by changing a thickness of the separation area. As the thickness of the separation area is increased, the mechanical strength is lowered. Therefore, the mechanical strength is also changed by changing the thickness. Specifically, the mechanical strength of the peripheral portion can be lowered by setting a thickness of a porous layer of the separation area larger in the peripheral portion than in the central portion of the base.

[0029] In order to obtain a suitable composite member which fails to be separated in a process prior to a process of separating the composite member and is securely separated in the separation process, the separation area is preferably formed by a plurality of layers different in mechanical strength. Especially, in the separation area comprising the plurality of layers, the thickness of a layer high in porosity is preferably less than the thickness of a layer low in porosity adjacent to a non-porous single-crystal semiconductor layer. A structure of each of the plurality of layers does not necessarily have to be steeply changed in an interface. Even if the strength or structure of each layer is continuously changed in the interface of the adjacent layers, separation is facilitated as compared with when the strength is uniform over the entire separation area.

[0030] In the separation area comprising the plurality of layers different in the mechanical strength, the layer high in porosity preferably has a higher porosity in the peripheral portion than in the vicinity of the central portion of the base.

[0031] In the separation area comprising the plurality of layers different in the mechanical strength, the porosity of a second layer with a high porosity can be made higher in the peripheral portion than in the central portion of the base substrate by making the thickness of a first layer with a small porosity larger in the peripheral portion than in the central portion of the base.

[0032] The present inventors have conducted experiments in which an anodization device is variously modified to form a good-quality porous layer. As a result, they have found that there is an Si wafer having an in-plane porosity distribution among a plurality of Si wafers subjected to a porous treatment using a certain mode of anodization device. Moreover, as a result of experiments in which samples are prepared by forming non-porous layers on porous layers and the non-porous layers are peeled off, it has been found that in some of the samples even the porous layer relatively low in porosity can be peeled off more easily than the layer relatively high in porosity. It is seen from the aforementioned two findings that, as in an embodiment described later, when the layer relatively high in porosity is ruptured or collapsed in the porous layers having the in-plane distribution of porosity, the layer relatively low in porosity is also easily ruptured, which is not much influenced by an absolute value of porosity.

[0033] Specifically, it has been found that when there is a layer relatively high in porosity in the peripheral portion of a member in which separation can easily be started, the separation is facilitated regardless of the absolute value of porosity, and the present invention has been developed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0034] **FIGS. 1A, 1B and 1C** are schematic sectional views of a composite member according to the present invention.

[0035] **FIGS. 2A and 2B** are top views of the composite member according to the present invention.

[0036] **FIGS. 3A and 3B** show in-plane distributions of mechanical strength of the composite member according to the present invention.

[0037] **FIG. 4** is view showing a state in which an anodization for use in the present invention is applied.

[0038] **FIG. 5** is a characteristic diagram of porosity of a semiconductor substrate according to the present invention.

[0039] **FIGS. 6A, 6B and 6C** are views showing a separation method of the composite member according to the present invention.

[0040] **FIG. 7** is a schematic view of a water jet device.

[0041] **FIG. 8** is a sectional view of the composite member of the present invention.

[0042] **FIG. 9** is a characteristic diagram showing a porous thickness and an anodization current.

[0043] **FIG. 10** is a characteristic diagram of porosity of a second layer relative to thickness of a first layer.

[0044] **FIG. 11** is a sectional view of the composite member according to an embodiment of the present invention.

[0045] **FIGS. 12A, 12B and 12C** are views showing a conventional preparation method of a semiconductor substrate.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0046] **FIGS. 1A to 1C** are sectional views of a composite member according to one embodiment of the present invention.

[0047] The composite member is formed by bonding a first base substrate **1** and a second base substrate **2** to each other, and a separation area **3** is formed inside. Here, the first base substrate **1** is bonded in such a manner that a layer **4** formed on the separation area **3** abuts on a surface of the second base substrate **2**, and a bonded interface **5** is formed. The separation area **3** has a portion **31** relatively high in mechanical strength and a weak portion **32**, and the mechanically weak portion **32** is positioned in a peripheral portion of the composite member (peripheral portion of the separation area). In the case of separating the composite member, since the portion **32** relatively low in mechanical strength is positioned in the peripheral portion of the composite member, the portion **32** is first cracked or collapsed, and the separation of the composite member is thus facilitated.

[0048] More specifically, **FIG. 1A** shows that the portion **32** of a porous material high in porosity is formed in the peripheral portion of the separation area **3** uniform in thickness, while the portion **31** of a porous material low in porosity is formed in a central portion, so that the portion **32** locally low in mechanical strength is provided in the peripheral portion. **FIG. 2A** shows positions of the mechanically strong and weak portions **31, 32** in the composite member as viewed from top. Numeral **7** denotes an orientation flat provided as required. Additionally, as shown in **FIG. 2B**, the mechanically weak portion **32** may be partially formed in the outer periphery of the composite member, instead of being formed in the entire outer periphery. The mechanically strong portion is larger than the weak portion. **FIG. 1B** shows the mechanically weak portion **32** formed in the peripheral portion by making non-uniform the thickness of the separation area **3** of a porous material uniform in porosity. Also in this case, as shown in **FIG. 2B**, the portion **32** may partially be formed in the outer periphery in the plane of the separation area **3**. **FIG. 1C** shows the mechanically weak portion **32** formed by implanting ions to form a portion having a large ion implantation amount in the peripheral portion. Also in this case, as shown in **FIG. 2B**, the mechanically weak portion **32** may partially be formed in the outer periphery by locally increasing the ion implantation amount. When hydrogen ions or rare gas ions are implanted, and a predetermined thermal treatment is performed, microcavities are generated. Therefore, a portion in which the ions are injected in high concentration may be formed into a porous portion high in porosity. The mechanically weak portion **32** may locally be formed by setting higher the porosity and thickness of the porous material than the other portions. Moreover, the mechanical strength of the ion implantated portion may be lowered by locally implant-

ing the ions into the separation area formed of the porous material and making fragile the porous material. That is, it is preferable to appropriately combine the characteristics of the structures shown in **FIGS. 1A to 1C.**

[0049] Preferably used as the first base substrate **1** of the present invention is an Si wafer or a plate-like semiconductor wafer of Ge, SiGe, SiC, GaAs, GaAlAs, InP, GaN or the like.

[0050] In addition to the same semiconductor wafer as that of the first base substrate **1**, a quartz glass, resin sheet or another insulating base, and a stainless steel or another metallic base substrate may be used as the second base substrate **2**.

[0051] The non-porous layer preferably comprises a single layer or a plurality of layers formed of a material selected from the group consisting of the same semiconductor materials as those for use in the first base. When the composite member is separated to prepare SOI substrate, a single-crystal semiconductor layer is preferable.

[0052] A layer **6** is preferably formed of an insulating material, a conductive material, or another material different from the material of the layer **4**.

[0053] Furthermore, the first and second base substrates are preferably bonded via an insulating layer or an adhesive layer.

[0054] **FIGS. 3A and 3B** are graphs relatively showing distributions of mechanical strength in the plane of the composite member.

[0055] A solid line **10** shows a mode in which the mechanical strength gradually increases from a left edge of an outer periphery LE1 toward a center 0 of the composite member, and a portion between positions LE2 and RE2 including the center 0 has the lowest mechanical strength. A dashed line **11** shows a mode in which the mechanical strength has an intermittent transition between an outer periphery (between outer peripheral edge LE1 and position LE2, between outer peripheral edge RE1 and position RE2) and a central portion (from position LE2 to RE2). A broken line **12** shows a mode in which the mechanical strength continuously increases from the outer peripheral edge LE1, RE1 toward the center 0, and the mechanical strength takes a maximum value only at the center 0.

[0056] In the present invention, it is preferable that the mechanical strength from a position 5 mm inside the outer peripheral edge of composite member to the outer peripheral edge of the separation area be locally lower than the mechanical strength in the central portion. Referring to **FIG. 3A**, the separation area is preferably formed as a thin layer in such a manner that the position 5 mm inside the outer peripheral edge of the composite member is between LE1 and LE2 and/or between RE2 and RE1.

[0057] Furthermore, when a large-diameter composite member is separated from its outer peripheral edge toward the center, there is a case where the central portion of the composite member cannot be separated as desired. In this case, a mechanically weak portion may locally be formed in the central portion. **FIG. 3B** shows an example of such mode, in which a portion between periphery and center, i.e., a donut-shaped portion M is high in mechanical strength.

[0058] When a porous layer is used as the separation area, the porosity of the mechanically weak peripheral portion is set to 20% or more, preferably 35% or more, and the upper limit of the porosity may be 80% or less.

[0059] The porosity of the mechanically strong central portion is not limited as long as it is lower than that of the peripheral portion, but may be selected preferably from the range of 5% to 35%, more preferably from the range of 5% to 20% in such a manner that the porosity becomes lower than that of the peripheral portion. When a difference in porosity is 5% or more, preferably 10% or more, a difference of mechanical strength sufficient for easily separating the composite member can be obtained in the peripheral portion and the central portion.

[0060] Additionally, in **FIG. 3B**, the portions M are mechanically strong. Therefore, when the separation area is formed of the porous material, the porosity of the portion M, i.e., the portion having the maximum value of mechanical strength may be set low in the range of 5% to 35%, preferably 5% to 20%, in the same manner as the porosity of the central portion of FIG. 3A.

[0061] The porosity of the center 0 in **FIG. 3B** needs to be higher than that of the portion M, and may appropriately be selected from the range of 20% to 80% to satisfy such relationship.

[0062] Here, the porosity P (%) of the porous material indicates a proportion of pore volume in an apparent volume of the porous material. The porosity is represented in the following equation using a density m of the porous material formed on the first base substrate and a density M of a non-porous material:

$$P=\{(M-m)\div M\}\times 100\ (\%) \tag{1}$$

[0063] Here, the density m of the porous material is obtained by dividing an apparent weight G of the porous material including pores by an apparent volume V of the porous material including the pores, and represented as follows:

$$m=G\div V \tag{2}$$

[0064] In practice, the porosity P of the porous layer of the base substrate in which only a depth d on the side of a surface has a porous layer structure can be obtained from the following equation using a weight A of the base substrate before the porous layer is formed thereon, a weight a of the base substrate after the porous layer is formed thereon, and a weight B of the base substrate after the porous layer is completely removed therefrom:

$$P=\{(A-a)\div(A-B)\}\times 100 \tag{3}$$

[0065] A method of preparing the composite member will next be described.

[0066] First, the first base substrate **1** of an Si wafer or the like is prepared, and the separation area **3** is formed on the surface of the first base substrate **1** or at a predetermined depth from the surface. Examples of the method for forming the separation area include a method of making the surface of the first base substrate **1** porous by anodization or the like and/or a method of implanting hydrogen ions, rare gas ions, or the like different from constituting elements of the base substrate to form an ion-implanted layer with a maximum ion implantation concentration at the predetermined depth from the surface of the first base substrate **1**. The mechani-

cally weak portion is formed in the peripheral portion by controlling the conditions of the anodization or ion implanting with procedures described later.

[0067] Subsequently, the non-porous layer **4** is formed on the separation area **3** if necessary, and the second base substrate is bonded. In the case of implanting the ions, a surface layer of the first base substrate constitutes the non-porous layer **4** as it is. When the surface of the first base substrate **1** is made porous, the layer **4** is formed thereon by sputtering or CVD. Subsequently, the non-porous layer **4** is bonded on the second base substrate of Si wafer or the like directly or via the insulating layer **6** as required. The composite member is thus completed.

[0068] In a method for forming the porous layer locally low in mechanical strength, the current density of anodization is changed in the plane. When the density of anodization current flowing into the peripheral portion of the semiconductor substrate is set high in the peripheral portion of the base, the thickness and/or porosity in the peripheral portion of the base substrate of the porous layer can be made higher than in the central portion of the base. To realize the current density distribution, for example, during the anodization, a sectional area, in which ion current flows, in an anodization liquid in the vicinity of the base substrate subjected to the formation is set larger than an area of the base substrate subjected to the formation. Thereby, a surface density of anodization current flowing into the base substrate peripheral portion may be set higher than a surface density of anodization current flowing into the base substrate center. Specifically, an anodization bath larger than the base substrate subjected to the formation is used, so that the ion current having a sectional area broader than the area of the base substrate is received by the base.

[0069] **FIG. 4** is a schematic view showing a device for use in anodization. In **FIG. 4**, numeral **101** denotes a DC power supply for the anodization, **102** denotes a cathode electrode, **103** denotes an anode electrode, and **104, 105** denote insulating supports for supporting the treated base substrate **1**. The base substrate **1** is engaged in recesses of the supports **104, 105**. Numeral **106** denotes an insulating bath bottom. The area of the electrode **102, 103** is about 1.2 to 3.0 times, preferably 1.3 to 2.0 times the area of the first base substrate **1**. In the structure, when ions flowing from the outside via the outer peripheral edge of the base substrate are collected in the base, more ions flow into the peripheral portion of the base, and the thickness and porosity of the porous layer of the peripheral portion can be raised.

[0070] Furthermore, while a plurality of stages of anodization are performed, the peripheral portion of the first porous layer is formed thicker than the central portion. Therefore, the porosity of the peripheral portion of the second porous layer formed later can be made higher than the porosity of the central portion.

[0071] When such distribution of flowing currents needs to be controlled more precisely, a current guide is provided in the vicinity of the base substrate subjected to the formation for controlling the distribution of ion currents flowing into the base substrate surface. When the ion current distribution is controlled, a distribution of thickness of the layer with a small porosity can be controlled.

[0072] When the layer formed by the ion implanting in which microcavities can be obtained is used as the separation area, the size or density of microcavities or the thickness of distributed microcavities can be increased by raising an ion implanting density, so that the mechanical strength of the area can be reduced.

[0073] Therefore, when the ion implantation amount of the base substrate peripheral portion is set larger than that of the base substrate central portion, the density of microcavities per unit volume of the base substrate peripheral portion is raised, and the porosity can be made higher than that of the base substrate central portion.

[0074] **FIG. 5** is a graph showing an in-plane distribution of porosity in a diametric direction of the porous material obtained in the method shown in **FIG. 4**.

[0075] As the porosity increases, the mechanical strength decreases. Therefore, **FIG. 5** shows a pattern vertically reverse to the pattern shown by the solid line **10** of **FIG. 3A**. When the ratio of the area of the electrode **102, 103** to the area of the base substrate is sufficiently large, a pattern shown by a solid line **15** is provided. When the ratio of the area of the electrode to the area of the base substrate is small, a tendency shown by a broken line **14** is provided. The porous material with a high porosity can thus be formed in the peripheral portion.

[0076] A technique for preparing a porous layer with a mechanical strength distribution shown in **FIG. 1A** or by the dashed line **11** of **FIG. 3A** will next be described. A first method is as follows:

[0077] A mask for ion implantation or photoresist pattern is provided only on the outer peripheral portion of the base substrate **1**, while boron ions are injected to the central portion. The base substrate having a low boron ion concentration locally in the outer periphery is subjected to anodization using an electrode having substantially the same area as that of the base, and the porous layer is prepared in which the outer peripheral portion has a high porosity while the central portion has a low porosity.

[0078] A second method is as follows:

[0079] The central portion of the base substrate excluding its outer peripheral portion is covered with wax or another mask resistant to the anodization, and general anodization is performed under a high current density to make porous the outer peripheral portion. Subsequently, the outer peripheral portion is masked, and the general anodization is performed under a low current density to make porous the central portion.

[0080] In a third method, after a uniform porous layer is formed by the general anodization, only the porosity of the outer peripheral portion is raised by ion implanting. When the distribution of ion implantation amount is controlled, the porous layer having the strength distribution as shown in **FIGS. 3A, 3B** can be formed with good controllability.

[0081] Additionally, in respect of the manufacture cost, the method shown in **FIG. 4** is more advantageous than these methods.

[0082] A method of preparing the composite member shown in **FIG. 1C** will next be described in more detail.

[0083] An Si wafer or another base subsirate is oxidized to form the insulating film **6**. Hydrogen or rare gas ions are implanted into the entire surface of the base substrate with

a predetermined acceleration voltage. The central portion excluding the outer peripheral portion is covered with a photoresist mask pattern, and the ions are again implanted into the outer peripheral portion with the same acceleration voltage. The separation area **3** having the mechanically weak portion **32** can be formed in this manner. After the mask pattern is removed, the insulating layer **6** is bonded onto the second base substrate **2**. Each of doses in first and second ion implanting operations is set in the range of $10^{12}cm^{-2}$ to $10^{17}cm^{-2}$, while a concentration of different atoms in the mechanically weak portion may be set in the range of $10^{17}cm^{-3}$ to $10^{23}cm^{-3}$.

[0084] A method of separating the composite member for use in the present invention will next be described. A mode of separating the composite member shown in **FIG. 1A** will be described as an example. As shown in **FIG. 6A**, an inner stress generated by thermal treatment or the like or an external force is used to separate the composite member. In the separation area **3**, since the peripheral portion **32** locally has a low mechanical strength, it is first collapsed or cracked. **FIG. 6A** shows that a wedge **110** is inserted and a force **111** is applied to separate the peripheral portion of the first base substrate **1** from the second base substrate **2**. Subsequently, as shown in **FIG. 6B**, the composite member is divided into two. When a residual layer **37** of the separation area **3** remaining on the non-porous layer **4** is relatively thick, the residual layer is removed by polishing or etching. Subsequently, thermal treatment (hydrogen annealing) is performed in an atmosphere of hydrogen if necessary. As shown in **FIG. 6C**, the base substrate **2** provided with the layer **4** having a smooth surface is obtained. For use in a solar battery, the residual layer does not need to be removed.

[0085] Examples of the separation method of the composite member usable in the present invention include pressurizing, pulling, shearing, wedge insertion, thermal treatment, vibration application, wire cutting, and various methods as disclosed in Japanese Patent Application Laid-open No. 7-302889. Additionally, as proposed in Japanese Patent Application No. 9-75498, the bonded first and second base substrates may be separated into a plurality of members in a separation area other than a bonded interface by spraying fluid or ejecting a jet of fluid to the vicinity of a side face of the separation area.

[0086] The jet of fluid for use in separation in the present invention can be realized by spouting pressurized fluid via a thin nozzle. A fluid jet method, as introduced in "Water Jet" Vol. 1, No. 1, page 4, can be used as a method for spouting a high-speed high-pressure flow of beams. In the fluid jet usable in the present invention, a liquid with a high pressure in the range of 100 to 3000 kgf/cm^2 pressurized by a high-pressure pump is spouted via a fine nozzle with a diameter of about 0.1 to 0.5 mm, so that ceramic, metal, concrete, resin, rubber, wood or another material can be cut (abrasive is added to water for a hard material), or worked. Additionally, a coating film of a surface layer can be removed, or member surfaces can be cleaned. In the conventional water jet method, it is a main effect to remove a part of the material as described above. Specifically, in the water jet cutting operation, a cutting width of a main member is removed, coating films are removed, or member surfaces are cleaned by removing unnecessary portions.

[0087] When water jet is used to form the fluid flow according to the present invention, the composite member can be separated by spouting the water jet to the side face of the separation area. In this case, the side face of the separation area is first exposed to the side face of the bonded base, and the water jet is directly spouted to the exposed portion or its peripheral portion. Then, the base substrate is separated into two without being damaged, while only the mechanically fragile separation area is removed by the water jet. Moreover, even if the side face of the separation area is not exposed beforehand for some reason, and the corresponding portion is covered with a thin layer like an oxide film, the layer covering the separation area is first removed with the water jet, before the base substrate can be separated with the water jet.

[0088] Moreover, an unused effect of the conventional water jet is used. Specifically, jet is spouted to a recess in the side face of the composite member to extend and collapse the structurally fragile separation area, so that the bonded wafer can be separated. In this case, chips of the separation area are hardly generated. Even if the separation area is formed of a material which cannot be removed by the jet, separation can be performed without using the abrasive or without damaging a separating surface.

[0089] The aforementioned effect is not an effect of cutting or polishing, and it can be expected to be an effect of wedge by the fluid as shown in **FIG. 6A**. This effect is much expected when a force is applied in a direction in which the separation area is pulled off by spouting the jet to a recess formed in the side face of the bonded base. In order to sufficiently fulfill the effect, the shape of the side face of the composite member is preferably concave, instead of being convex.

[0090] **FIG. 7** is a schematic perspective view showing an example of a water jet device for use in the method of manufacturing the semiconductor substrate in the present invention. In **FIG. 7**, a composite member **1** is formed by integrally bonding two Si wafers, and the separation area **3** is provided inside. Supports **403, 404** are provided on the same rotating shaft for adsorbing/fixing the composite member **1** by a vacuum chuck. Furthermore, the support **404** is connected to a support base substrate **409** via a bearing **408**, and its rear is directly connected to a speed control motor **410**, so that the support **404** can be rotated at an arbitrary speed. Moreover, the support **403** is connected to the support base substrate **409** via a bearing **411**, and its rear is connected to the support base substrate **409** via a compression spring **412**, so that a force is applied in a direction in which the support **403** is detached from the composite member **1**.

[0091] First, the composite member **1** is set in accordance with a positioning pin **413**, and adsorbed/held by the support **404**. Since the composite member **1** is positioned by the positioning pin **413** of a tool **407**, the central portion of the composite member **1** can be held. Subsequently, the support **403** is advanced toward the left along the bearing **411** until the composite member **1** is adsorbed/held. Then, a force exerted toward the right is applied to the support **403** by the compression spring **412**. In this case, a returning force of the compression spring **412** and a force of the support **403** for sucking the composite member **1** are balanced to prevent the support **403** from being detached from the composite member **1** by the force of the compression spring **412**.

[0092] Subsequently, water is fed to a water jet nozzle **402** from a water jet pump **414**, and water is continuously

spouted for a constant time until spouted water is stabilized. When the water is stabilized, a shutter **406** is opened to spout the water (hereinafter referred to as the jet water) to the side face of the composite member **1** from the water jet nozzle **402**. In this case, the composite member **1** and the support **403** are rotated by rotating the support **404**. Since the jet water is applied near the center of the thickness of the side face of the composite member **1**, the composite member **1** is pushed/extended into two toward its center from its outer peripheral portion, the separation area relatively weak in the composite member **1** is collapsed, and the composite member is finally separated into two pieces.

[0093] As described above, the jet water is applied uniformly to the composite member **1**. Moreover, while the support **403** supports the composite member **1**, the force is exerted toward the right. Therefore, the separated pieces of the composite member **1** do not slide on each other.

[0094] Alcohol or another organic solvent; hydrofluoric acid, nitric acid or another acid; potassium hydroxide or another alkali; or another liquid having a function of selectively etching the separation area can be used as the fluid instead of water. Furthermore, usable as the fluid is air, nitrogen gas, carbonic acid gas, rare gas or another gas. Gas or plasma having a function of etching the separation area can also be used. In the separation method of the composite member introduced in the preparation method of the semiconductor substrate, pure water from which impurity metals or particles are removed as much as possible, super pure water or another water with high purity is preferably used. Moreover, a completely low-temperature process is introduced. Therefore, even if the jet fluid other than pure water is used, the impurities or particles can be removed by cleaning after the separation.

[0095] In the method of spraying the fluid as described above, the vicinity of the separation area of the composite member is preferably recessed in a concave shape for receiving the fluid to produce a force in a direction in which the separation area is pushed/extended. When the composite member formed by bonding two base substrates via the separation area is separated at the separation area, the aforementioned structure can easily be realized by chamfering edges of the bases.

[0096] The water jet or another fluid flow, pressurizing, pulling, shearing, wedge insertion, thermal treatment, vibration application, wire cutting, and other various methods may be used to apply a separating force to the separation area formed beforehand in the composite member and to separate the composite member into two. In this case, the separation is performed by collapsing the mechanically fragile portion of the separation area. When the fluid is spouted to the vicinity of the separation area, the mechanically fragile separation area is removed or collapsed by the fluid flow. When the fluid is used, however, basically the separation area is removed while the other non-fragile portions remain without being collapsed. As a result, the separation can advantageously be performed without damaging any portion that is used after the separation. In any of the methods, however, unless the separation area is sufficiently weak, it cannot be collapsed. For example, there is a case where the separation area cannot be collapsed or removed with the fluid flow with a predetermined pressure.

[0097] To solve the problem, when the pressure of the fluid is raised, not only the separation area but also the other portions are collapsed. For example, when the bonded base substrate is separated, the plate-like first or second base substrate is cracked. To prevent this, when the pressure of the fluid is lowered, however, the separation cannot be performed.

[0098] In most of the separation methods, in the initial separation stage, a solid wedge needs to be pushed into the vicinity of the surface of the separation area formed in the composite member, e.g., the separation area of the portion formed in the peripheral portion of the disc-shaped bonded base. In many cases, the separation needs to proceed from the surface. While the separation fails to proceed, the portion close to the surface has a small area to which the separating force is applied. A problem is therefore caused that a surface density of force has to be raised. This is because the separating force can be applied to the separated surface, but no separating force can be applied to the surface not yet separated. When the separation proceeds, the area to which the separating force can be applied is enlarged. Therefore, even when the separating force applied to the separating surface is increased to facilitate the separation, the surface density is decreased, and the base substrate can easily be prevented from being broken (cracked or otherwise) by the separation.

[0099] In order to facilitate the separation, in the initial stage of separation, the mechanical strength may be lowered by raising the porosity of the porous layer of the separation area, increasing the thickness of the porous layer, or increasing the ion implanting amount to increase the amount of generated microcavities. When the strength is excessively lowered, however, a disadvantage is caused that in the process of forming the composite member, the separation area is collapsed before the separation process.

[0100] As a result of intensive researches, the present inventors have found that in order to avoid the aforementioned disadvantages, the mechanical strength of the separation area is changed in parallel with the bonded face, and the mechanical strength particularly of the portion of the separation area close to the bonded base substrate surface, e.g., the peripheral portion is set lower than that of the base substrate central portion.

[0101] In the initial stage of separation, since the area of the separated face is small and the separating force cannot be increased, the mechanical strength of the separation area is reduced, so that the separation is advanced with a small force. This is realized by reducing the mechanical strength of the separation area in the vicinity of the base substrate peripheral portion. Peeling during the process is prevented by setting the mechanical strength of the separation area higher in the base substrate central portion than in the peripheral portion.

[0102] In this case, when the separation is advanced to the central portion, the separated area is broad. Therefore, even when the surface density of the separating force is reduced, the entire separating force is increased, and the separation can be advanced. Such effect is fulfilled regardless of the separation method, but the method of spouting the fluid flow to the separation area is most preferable for applying the separating force relatively uniformly to the entire separated face to prevent the base substrate from being broken.

[0103] In order to broaden the range of conditions for performing a stable separation to securely separate the base

substrate without damaging it, as shown in **FIG. 8**, the separation area **3** is preferably formed of a plurality of layers or areas **22**, **23** different in mechanical strength. In this case, the mechanical strength of the peripheral portion can relatively easily be made smaller as compared with that of the central portion of the base. When the separation area has a lamination structure of the layer **23** small in porosity (hereinafter referred to as the first porous layer) and the layer **22** large in porosity (hereinafter referred to as the second porous layer), the layer **23** small in porosity is first formed by the anodization, and subsequently the anodization current is increased to similarly form the layer **22** large in porosity by the anodization.

[0104] As a result of intensive researches, the present researchers have found that the porosity of the second porous layer **22** is not determined only by the magnitude of the current, and it also depends on the thickness or porosity of the first porous layer **23**. When the anodization current of the second porous layer **22** is set equal, but the first porous layer **23** is thick or low in porosity, then the porosity of the second porous layer **22** tends to be increased. Therefore, for example, as the thickness of the first porous layer **23** is reduced, the anodization current of the second porous layer **22** needs to be raised in order to keep high the porosity of the second porous layer **22**. This relationship is shown in **FIG. 9**.

[0105] If the anodization current of the second porous layer is kept constant, and the thickness of the first porous layer is changed, the porosity of the second porous layer is influenced. Such relationship is shown in **FIG. 10**. It is apparent that after the first porous layer is formed, the second porous layer cannot be formed independently, and the characteristics of the first porous layer exert an influence on the porosity of the second porous layer. A detailed mechanism of such phenomenon is not completely explicated. As described later, however, F^- ions in a formation liquid are necessary for forming porous Si. When the F^- ions are consumed in a pore forming portion at a tip end of a pore, new F^- ions need to be supplied to the tip end of the pore from a surface of the porous Si through the pore.

[0106] It is supposed that such effective transportability of the F^- ions in the pore by electric field or diffusion depends on the pore size or length of the first layer, i.e., the thickness of the first layer. Specifically, the first porous layer itself formed by the anodization limits the transport of ions necessary for forming the subsequent porous layer.

[0107] Therefore, the formed first porous layer serves as a layer for limiting the effective transportability of the F^-ions necessary for forming the subsequent porous layer. When the anodization current is constant, the formation is advanced to form a sufficient thickness without largely changing the porosity. This is because a pore of a size determined by a balance between consumption and supply of F^-ions is formed at a constant current, but if the current is increased halfway, the balance between consumption and supply of the F^- ions is changed by the existence of the formed porous layer, and the pore size is largely changed.

[0108] When the thickness of the first layer is increased and the effective transportability of F^- ions transported through the layer is lowered, the concentration of F^- ions in the tip end of the pore is decreased, and an ion lacking layer is spread in the formation liquid in the pore. Therefore, a portion in which a potential barrier of an interface between formation liquid and Si single-crystal surface in the pore is lowered is extended. In the portion Si is etched, and the pore size may be increased.

[0109] In practice, even when the anodization current is simply increased, the porosity is not much increased unless the transportability limiting layer is formed on the Si surface. This rather increases the formation rate. Therefore, in order to largely change the porosity by increasing the anodization current, the layer for limiting the transportability of the F^- ions is necessary between porosity increasing layer and formation liquid. If the thickness of the first porous layer can be increased in the periphery of the base, the porosity of the second porous layer in the corresponding portion can be larger than the porosity of the second layer in a central portion where the first layer is thin. Thereby, the mechanical strength of the separation area of the base substrate peripheral portion can be reduced.

[0110] The present invention is characterized in that when the mechanism of the anodization is well used as described above to form the separation area comprising a plurality of layers or areas different in the mechanical strength, the porosity of the layer **22** large in porosity can be made higher in the peripheral portion than in the central portion of the base substrate by increasing the thickness of the layer **23** small in porosity in the peripheral portion rather than in the central portion of the base.

[0111] As described above, the porous layer can be formed on the wafer by the anodization using the simple device shown in **FIG. 4**. The layer with a small porosity can be formed thicker in the base substrate peripheral portion than in the base substrate central portion, which can make higher the porosity of the subsequently formed layer with a large porosity in the base substrate peripheral portion than in the base substrate central portion. When the distribution of incoming current needs to be controlled more precisely, the current guide is provided in the vicinity of the base substrate subjected to the formation for controlling the distribution of ion currents flowing into the base substrate surface. When the ion current distribution is controlled, the distribution of thickness of the layer with a small porosity can be controlled.

[0112] Moreover, the water jet injection device for separating the wafer and the thin-film semiconductor from the composite member comprising the first and second base substrates has been described above with reference to **FIG. 7**.

[0113] An example of the bonded base substrate usable in the method of the present invention will be described in more detail with reference to **FIG. 8**. In the example, as shown in **FIG. 8**, the separation area **3** has a double layer structure comprising the first porous layer **23** with a low porosity and the second porous layer **22** with a higher porosity and a lower mechanical strength. In the present invention, for the second porous layer **22**, its porosity or thickness may be set higher in the vicinity of the base substrate peripheral portion than in the central portion. During the separation, cracks are generated in the second porous layer **22** in a position different from the bonded interface or in the interface. The second porous layer **22** has a low mechanical strength. Therefore, when a force is applied in a direction in which a first base substrate **21** and

a second base substrate **27** are separated from each other, only the second porous layer **22** is collapsed and the base substrates are separated. In this case, when a layer **4** of non-porous single-crystal Si is formed, the first porous layer **23** is necessary as a protective layer for suppressing the generation of crystal defects or for preventing the layer **4** from being collapsed in the separation process. When the porosity is not much increased, the separation can be performed without forming the second porous layer **22**, but the second porous layer **22** is preferably formed to provide a good yield.

[0114] Embodiments of the present invention will next be described in more detail.

EXAMPLE 1

[0115] A first P-type (or N-type) (**100**) single-crystal Si substrate with a thickness of 625 μm, a specific resistance of 0.01 Ω·cm and a diameter of eight inches was used, and anodization was performed in HF solution. A formation bath was prepared in such a manner that a sectional area of a plane parallel with a formation electrode of an anodization layer and the Si single-crystal base substrate was about twice an area of the Si base, and the formation bath was used.

[0116] Anodization conditions are as follows:

[0117] anodization current: 2.6 A

[0118] anodization solution:HF:H_2O:C_2H_5OH=1:1:1

[0119] time: 11 minutes

[0120] The thickness of a central portion of a porous layer of the base substrate subjected to the formation was about 12 μm and the porosity of the central portion was about 20%, while the thickness of the porous layer of a peripheral portion was about 19 μm at maximum and the porosity was 30%. The pore size of the peripheral portion of the base substrate prepared under these conditions can be measured by observation with an electronic microscope. It is apparent that the pore size is larger in a portion deep from a surface than in the central portion. However, for the central portion or the peripheral portion, no remarkable difference in pore size can be found in the vicinity of the surface of the porous layer. This is essential for the subsequent process, in which Si single crystal having less defects is epitaxially developed into a porous layer structure.

[0121] The substrate was cleaned with hydrofluoric acid at 400° C. in the atmosphere of oxygen, then oxidized for one hour. Inner walls of pores of the porous Si were covered with a thermally oxidized film through the oxidization. After thermal treatment was performed at 950° C. in the atmosphere of hydrogen, single-crystal Si epitaxially grew by 0.3 μm on the porous Si by CVD method under the following conditions:

[0122] source gas: SiH_4

[0123] carrier gas: H_2

[0124] temperature: 900° C.

[0125] pressure: 1×10^{-2} Torr

[0126] growth rate: 3.3 nm/sec

[0127] Furthermore, 100 nm of SiO_2 layer was formed on a surface of the epitaxial Si layer by the thermal oxidization.

[0128] After the surface of the SiO_2 layer and a surface of a separately prepared Si substrate were overlapped and contacted with each other, thermal treatment was performed at 1180° C. for five minutes to perform bonding. When the composite member was set in the device shown in **FIG. 7**, and water jet injection was performed with a water pressure of 1000 kgf/cm^2 and a diameter of 0.15 mm, the porous Si layer was collapsed, the wafer was effectively divided in two, and the porous Si was exposed to a separated face of two Si substrates. Subsequently, the porous Si layer was selectively etched with etching liquid of HF/H_2O_2/C_2H_5OH. The porous Si was selectively etched and completely removed. The etching rate of the non-porous Si single crystal to the etching liquid is remarkably low, and the etching amount in the non-porous layer can practically be ignored. Specifically, a single-crystal Si layer having a thickness of 0.2 μm could be formed on the oxidized Si film. The single-crystal Si layer underwent no change even by the selective etching of the porous Si. Resulting SOI substrate was thermally treated in the atmosphere of hydrogen.

[0129] As a result of the observation of a cross section by a transmission electronic microscope, it was confirmed that no crystal defect was introduced to the Si layer and that good crystallizability was kept. Even when no oxide film was formed on the surface of the epitaxial Si layer, similar results were obtained. The first Si single-crystal substrate was reused as a first Si single-crystal substrate for obtaining another SOI substrate, by removing residual porous Si therefrom.

EXAMPLE 2

[0130] A first P-type (or N-type) (**100**) single-crystal Si substrate with a thickness of 625 μm, a specific resistance of 0.01 Ω·cm and a diameter of eight inches was used, and anodization was performed in HF solution. A formation bath was prepared in such a manner that a sectional area of a plane parallel with a formation electrode of an anodization layer and the Si single-crystal base substrate was about twice an area of the Si base, and was used.

[0131] Anodization conditions are as follows:

[0132] anodization current: 2.6 A

[0133] anodization solution:HF:H_2O:C_2H_5OH=1:1:1

[0134] time: 11 minutes

[0135] The thickness of a central portion of a first porous layer of the base substrate subjected to the formation was about 12 microns, and the porosity of the central portion was about 20%. The thickness of the porous layer of a peripheral portion was about 19 μm at maximum and the porosity was 30%. Subsequent to the formation of the first layer, the formation of a second layer was performed under the following conditions:

[0136] anodization current: 8 A

[0137] anodization solution:HF:H_2O:C_2H_5OH=1:1:1

[0138] time: two minutes

[0139] When the formation of the second layer was performed under the above conditions after the first layer was formed, the thickness of the center of the second layer was about two microns, and the porosity was about 40%. In the

peripheral portion of the base, however, the porosity was about 55% at maximum, and its thickness was less than two microns.

[0140] However, for the central portion or the peripheral portion, no remarkable difference in pore size can be found in the vicinity of the surface of the first porous layer. This is essential for the subsequent process, in which Si single crystal having less defects is epitaxially developed into a porous layer structure.

[0141] The substrate was oxidized at 400° C. in the atmosphere of oxygen for one hour. Inner walls of pores of the porous Si were covered with a thermally oxidized film through the oxidization. Subsequently, after cleaning was performed with HF solution and thermal treatment was performed in the atmosphere of hydrogen, single-crystal Si epitaxially grew by 0.3 μm on the porous Si by CVD method. The growing conditions were as follows:

[0142] source gas: SiH_4

[0143] carrier gas: H_2

[0144] temperature: 900° C.

[0145] pressure: 1×10^{-2} Torr

[0146] growth rate: 3.3 nm/sec

[0147] Furthermore, 100 nm of SiO_2 layer was formed on a surface of the epitaxial Si layer by the thermal oxidization.

[0148] After the surface of the SiO_2 layer and a surface of a separately prepared Si substrate were overlapped and contacted with each other, thermal treatment was performed at 1180° C. for five minutes to perform bonding. A cross section of resulting composite member is diagrammatically shown in **FIG. 11**. The porous layer was exposed to wafer edges, the porous Si was etched to some degree, and a plate as sharp as a razor blade was inserted to the corresponding portion. Then, the porous Si layer was ruptured, the wafer was divided into two, and the porous Si was exposed. Subsequently, the porous Si layer was selectively etched with etching liquid of $HF/H_2O_2/C_2H_5OH$. The porous Si was selectively etched and completely removed. The etching rate of the non-porous Si single crystal to the etching liquid is remarkably low, and the etching amount in the non-porous layer provides a practically ignorable decrease of thickness. Specifically, a single-crystal Si layer having a thickness of 0.2 μm could be formed on the oxide Si film. The single-crystal Si layer underwent no change even by the selective etching of the porous Si. Resulting SOI substrate was thermally treated in the atmosphere of hydrogen.

[0149] As a result of the observation of a cross section by a transmission electronic microscope, it was confirmed that no crystal defect was introduced to the Si layer and that good crystallizability was kept. Even when no oxidized film was formed on the surface of the epitaxial Si layer, similar results were obtained. The first Si single-crystal substrate was reused as a first Si single-crystal substrate by removing residual porous Si therefrom.

EXAMPLE 3

[0150] A first P-type (or N-type) (**100**) single-crystal Si substrate with a thickness of 625 μm, a specific resistance of 0.01 Ω-cm and a diameter of eight inches was used, and anodization was performed in HF solution. A formation bath was prepared in such a manner that a sectional area of a plane parallel with a formation electrode of an anodization layer and the Si single-crystal base substrate was about twice an area of the Si base, and was used.

[0151] Anodization conditions are as follows:

[0152] anodization current: 2.6 A

[0153] anodization solution:$HF:H_2O:C_2H_5OH=1:1:1$

[0154] time; 11 minutes

[0155] The thickness of a central portion of a first porous layer of the base substrate subjected to the formation was about 12 microns, and the porosity of the central portion was about 20%. The thickness of the porous layer of a peripheral portion was about 19 μm at maximum and the porosity was 30%. Subsequent to the formation of the first layer, the formation of a second layer was performed under the following conditions:

[0156] anodization current: 8 A

[0157] anodization solution:$HF:H_2O:C_2H_5OH=1:1:1$

[0158] time: two minutes

[0159] When the formation of the second layer was performed under the above conditions after the first layer was formed, the thickness of the center of the second layer was about two microns, and the porosity was about 40%. In the peripheral portion of the base, however, the porosity was about 55% at maximum, and its thickness was less than two microns.

[0160] However, for the central portion or the peripheral portion, no remarkable difference in pore size can be found in the vicinity of the surface of the first porous layer. This is essential for the subsequent process, in which Si single crystal having less defects is epitaxially developed into a porous layer structure.

[0161] The substrate was oxidized at 400° C. in the atmosphere of oxygen for one hour. Inner walls of pores of the porous Si were covered with a thermally oxidized film through the oxidization. After cleaning was performed with HF solution and thermal treatment was performed in the atmosphere of hydrogen, single-crystal Si epitaxially grew by 0.3 μm on the porous Si by CVD method. The growing conditions were as follows:

[0162] source gas: SiH_4

[0163] carrier gas: H_2

[0164] temperature: 900° C.

[0165] pressure: 1×10^{-2} Torr

[0166] growth rate: 3.3 nm/sec

[0167] Furthermore, 100 nm of SiO_2 layer was formed on a surface of the epitaxial Si layer by the thermal oxidization.

[0168] After the surface of the SiO_2 layer and a surface of a separately prepared Si substrate were overlapped and contacted with each other, thermal treatment was performed at 1180° C. for five minutes to perform bonding. The composite member as shown in **FIG. 11** was thus obtained. For wafer side faces, water jet injection was performed with a water pressure of 300 kgf/cm^2 and a diameter of 0.1 mm. Then, the porous Si layer was ruptured, the wafer was

effectively divided into two, and the porous Si was exposed. Subsequently, the porous Si layer was selectively etched with etching liquid of $HF/H_2O_2/C_2H_5OH$. The porous Si was selectively etched and completely removed. The etching rate of the non-porous Si single crystal to the etching liquid is remarkably low, and the etching amount in the nonporous layer provides a practically ignorable decrease of thickness. Specifically, a single-crystal Si layer having a thickness of 0.2 μm could be formed on the oxide Si film. The single-crystal Si layer underwent no change even by the selective etching of the porous Si. Resulting SOI substrate was thermally treated in the atmosphere of hydrogen.

[0169] As a result of the observation of a cross section by a transmission electronic microscope, it was confirmed that no crystal defect was introduced to the Si layer and that good crystallizability was kept. Even when no oxidized film was formed on the surface of the epitaxial Si layer, similar results were obtained. The first Si single-crystal substrate was reused as a first Si single-crystal substrate by removing residual porous Si therefrom.

EXAMPLE 4

[0170] A first P-type or N-type (**100**) single-crystal Si substrate with a thickness of 625 μm, a specific resistance of 0.01 Ω-cm and a diameter of eight inches was used, and anodization was performed in HF solution. A formation bath was prepared in such a manner that a sectional area of a plane parallel with a formation electrode of an anodization layer and the Si single-crystal base substrate was about 1.3 times an area of the Si base, and was used.

[0171] Anodization conditions are as follows:

[0172] anodization current: 2.6 A

[0173] anodization solution:$HF:H_2O:C_2H_5OH=1:1:1$

[0174] time: 11 minutes

[0175] The thickness of a central portion of a first porous layer of the base substrate subjected to the formation was about six microns, and the porosity of the central portion was about 20%. The thickness of the porous layer of a peripheral portion was about eight μm at maximum and the porosity was 25%. Subsequent to the formation of the first layer, the formation of a second layer was performed under the following conditions:

[0176] anodization current: 12 A

[0177] anodization solution:$HF:H_2O:C_2H_5OH=1:1:1$

[0178] time: one minute

[0179] For the central portion or the peripheral portion, no remarkable difference in pore size can be found in the vicinity of the surface of the first porous layer. This is essential for the subsequent process, in which Si single crystal having less defects is epitaxially developed into a porous layer structure.

[0180] The substrate was oxidized at 400° C. in the atmosphere of oxygen for one hour. Inner walls of pores of the porous Si were covered with a thermally oxidized film through the oxidization. After cleaning was performed with HF solution and thermal treatment was performed in the atmosphere of hydrogen, single-crystal Si epitaxially grew by 0.3 μm on the porous Si by CVD method. The growing conditions were as follows:

[0181] source gas: SiH_4

[0182] carrier gas: H_2

[0183] temperature: 900° C.

[0184] pressure: 1×10^{-2} Torr

[0185] growth rate: 3.3 nm/sec

[0186] Furthermore, 100 nm of SiO_2 layer was formed on a surface of the epitaxial Si layer by the thermal oxidization.

[0187] After the surface of the SiO_2 layer and a surface of a separately prepared Si substrate were overlapped and contacted with each other, thermal treatment was performed at 1180° C. for five minutes to perform bonding. The porous layer was exposed to wafer edges and, instead of etching the porous Si to some decree, water jet injection was performed with a water pressure of 300 kgf/cm^2 and a diameter of 0.1 mm. Then, the porous Si layer was ruptured, the wafer was effectively divided into two, and the porous Si was exposed. Subsequently, the porous Si layer was selectively etched with etching liquid of $HF/H_2O_2/C_2H_5OH$. The porous Si was selectively etched for a shorter time than in the third example, and completely removed. The etching rate of the non-porous Si single crystal to the etching liquid is remarkably low, and the etching amount in the non-porous layer provides a practically ignorable decrease of film thickness. Specifically, a single-crystal Si layer having a thickness of 0.2 μm could be formed on the oxidized Si film. The single-crystal Si layer underwent no change even by the selective etching of the porous Si. Resulting SOI substrate was thermally treated in the atmosphere of hydrogen.

[0188] As a result of the observation of a cross section by a transmission electronic microscope, it was confirmed that no crystal defect was introduced to the Si layer and that good crystallizability was kept. Even when no oxidized film was formed on the surface of the epitaxial Si layer, similar results were obtained. The first Si single-crystal substrate was used again as a first Si single-crystal substrate by removing residual porous Si therefrom.

EXAMPLE 5

[0189] A first P-type (or N-type) (**100**) single-crystal Si substrate with a thickness of 625 μm, a specific resistance of 0.01 Ω-cm and a diameter of eight inches was used, and anodization was performed in HF solution. A formation bath was prepared in such a manner that a sectional area of a plane parallel with a formation electrode of an anodization layer and the Si single-crystal base substrate was about 1.3 times an area of the Si base, and was used.

[0190] Anodization conditions are as follows:

[0191] anodization current: 2.6 A

[0192] anodization solution:$HF:H_2O:C_2H_5OH=1:1:1$

[0193] time: 11 minutes

[0194] The thickness of a central portion of a first porous layer of the base substrate subjected to the formation was about six microns, and the porosity of the central portion was about 20%. The thickness of the porous layer of a peripheral portion was about eight μm at maximum and the porosity was 25%. Subsequent to the formation of the first layer, the formation of a second layer was performed under the following conditions:

[0195] anodization current: 12 A

[0196] anodization solution:$HF:H_2O:C_2H_5OH=1:1:1$

[0197] time: one minute

[0198] For the central portion or the peripheral portion, no remarkable difference in pore size can be found in the vicinity of the surface of the first porous layer. This is essential for the subsequent process, in which Si single crystal having less defects is epitaxially developed into a porous layer structure.

[0199] The substrate was oxidized at 400° C. in the atmosphere of oxygen for one hour. Inner walls of pores of the porous Si were covered with a thermally oxidized film through the oxidization. After cleaning was performed with HF solution and thermal treatment was performed in the atmosphere of hydrogen, single-crystal Si epitaxially grew by 0.3 μm on the porous Si by CVD method. The growing conditions were as follows:

[0200] source gas: SiH_4

[0201] carrier gas: H_2

[0202] temperature: 900° C.

[0203] pressure: 1×10^{-2} Torr

[0204] growth rate: 3.3 nm/sec

[0205] Furthermore, 100 nm of SiO_2 layer was formed on a surface of the epitaxial Si layer by the thermal oxidization.

[0206] After the surface of the SiO_2 layer and a surface of a separately prepared Si substrate were overlapped and contacted with each other, thermal treatment was performed at 1180° C. for five minutes to perform bonding. The porous layer was exposed to wafer edges, and the porous Si was etched to some degree. A multiplicity of bonded base substrates prepared as described above were simultaneously submerged in a water bath of an ultrasonic radiation device. When about 50 kHz of ultrasonic waves were radiated, porous Si layers of all the bonded base substrates were ruptured, each wafer was divided into two, and the porous Si was exposed. Subsequently, the porous Si layer was selectively etched with etching liquid of $HF/H_2O_2/C_2H_5OH$. The porous Si was selectively etched in a shorter time than in the third example, and completely removed. The etching rate of the non-porous Si single crystal to the etching liquid is remarkably low, and the etching amount in the non-porous layer provides a practically ignorable decrease of thickness. Specifically, a single-crystal Si layer having a thickness of 0.2 μm could be formed on the oxidized Si film. The single-crystal Si layer underwent no change even by the selective etching of the porous Si.

[0207] As a result of the observation of a cross section by a transmission electronic microscope, it was confirmed that no crystal defect was introduced to the Si layer and that good crystallizability was kept. Even when no oxidized film was formed on the surface of the epitaxial Si layer, similar results were obtained. The first Si single-crystal substrate was used again as a first Si single-crystal substrate by removing residual porous Si therefrom.

EXAMPLE 6

[0208] As an insulating layer, 200 nm of oxidized film (SiO_2 layer) was formed on a surface of a first single-crystal Si substrate.

[0209] A first ion implantation was performed from the surface of the first substrate in such a manner that projection range fell in the Si substrate. In this manner, a layer serving as a separation area was formed as a distorted layer by a microcavity layer or a layer with a high concentration of ions injected therein in a depth of the projection range. Subsequently, under substantially the same conditions as those of the first ion implantation, ion implantation was again performed in the range of a 10 mm wide peripheral portion of the substrate. Thereby, the ion implantation amount of the peripheral portion was about twice that of the central portion.

[0210] After the ion implantation, a surface of the SiO_2 layer and a surface of a second Si substrate separately prepared were overlapped and contacted with each other, then thermal treatment was performed at 600° C. to perform bonding.

[0211] While the central portion of the substrate bonded as described above was held, and the substrate was rotated around a central axis, water jet injection was performed from the peripheral portion in parallel with a bonded face under a water pressure of 300 kgf/cm^2 and a diameter of 0.1 mm. Then, the separation area was collapsed and the wafer was remarkably effectively separated.

[0212] As a result, the SiO_2 layer, surface single-crystal layer and a part of separation layer originally formed on the surface of the first substrate were transferred to the second substrate. A remaining part of the separation layer was left on the surface of the first substrate. After the separation, the second substrate was annealed at 1000° C. Thereafter, the separation layer transferred to the second substrate was polished and removed with CMP device, and its surface was smoothed.

[0213] Specifically, a single-crystal Si layer having a thickness of 0.2 μm could be formed on the oxidized Si film. For all in-plane faces, the thickness of the single-crystal Si layer formed on the insulating layer as described above was measured in 100 points or positions. As a result, the uniformity of the film thickness was 201 nm±7 nm.

[0214] As a result of the observation of a cross section by a transmission electronic microscope, it was confirmed that no new crystal defect was introduced to the Si layer and that good crystallizability was kept.

[0215] Furthermore, after thermal treatment was performed at 1100° C. in hydrogen for one hour, surface roughness was evaluated with an interatomic force microscope. As a result, an average square roughness in 50 μm square was about 0.2 nm, which was equivalent to the roughness of an ordinarily marketing Si wafer.

[0216] Even when the oxidized film was formed on only the surface of the second substrate or on the surfaces of the epitaxial layer and second substrate, similar results were obtained.

[0217] Moreover, when the separation layer remaining on the first substrate is regenerated by etching or surface polishing, and hydrogen annealing or another surface treatment is further applied if necessary, the substrate can be used again as a first or second substrate.

[0218] In the example, the surface area of the Si wafer is transferred to the second substrate via the separation layer

by the ion implantation, but an epitaxial wafer may be used to transfer the epitaxial layer to the second substrate via the separation layer by the ion implantation. Moreover, after the ion implantation of the example, a surface SiO_2 is removed, an epitaxial layer is formed, SiO_2 is further formed, then the bonding process is performed, so that the epitaxial layer may be transferred to the second substrate via the separation by the ion implantation. In the latter case, the surface area of the Si wafer is also transferred.

[0219] In the aforementioned examples for separating the composite member, even when the separating force is raised, the separation proceeds toward the inside from edges of the bonded base substrates without breaking one or both of the halfway separated bases. Moreover, the separated first base substrate may be used again as a semiconductor base substrate for obtaining the next SOI substrate.

[0220] Additionally, one of the separated base substrates can be reused in preparing bonded bases, which enhances a yield of base substrate separation.

[0221] Moreover, particles generated by the collapsed separation area can be prevented from causing contamination in the process. Furthermore, when the separation is performed by another method using no fluid, the separation yield can be enhanced.

[0222] Additionally, a suitable composite member can be prepared in such a manner that when the base substrate is separated from the separation area formed inside the bonded semiconductor base substrate or another composite member, separation does not occur before the separation process, and separation is securely performed in the separation process.

What is claimed is:

1. A composite member comprising a separation area inside, wherein mechanical strength of the separation area is non-uniform along a surface of the composite member and wherein portions different from each other in porosity, thickness or ion implantation amount are formed in the separation area such that a mechanical strength of a peripheral portion of the separation area is locally low.

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IX. RELATED PROCEEDINGS APPENDIX

There are no related proceedings.